

SUB-NYQUIST RATE SAMPLING DATA ACQUISITION SYSTEMS BASED ON  
COMPRESSIVE SENSING

A Dissertation

by

XI CHEN

Submitted to the Office of Graduate Studies of  
Texas A&M University  
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

May 2011

Major Subject: Electrical Engineering

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## ABSTRACT

Sub-Nyquist Rate Sampling Data Acquisition Systems Based on Compressive Sensing.

(May 2011)

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Chair of Advisory Committee: Dr. Sebastian Hoyos

This dissertation presents the fundamental theory and design procedure of the sub-Nyquist rate sampling receiver front-end that exploits signal sparsity by employing Compressive Sensing (CS) techniques. The CS receiver serves as an Analog-to-Information Conversion (AIC) system that works at sampling rates much lower than the Nyquist rate. The performance of a parallel path CS front-end structure that employs current mode sampling techniques is quantified analytically. Useful and fundamental design guidelines that are unique to CS are provided based on the analytical tools. Simulations with IBM 90nm CMOS process verify the theoretical derivations and the circuit implementations. Based on these results, it is shown that instantaneous receiver signal bandwidth of 1.5 GHz and 44 dB of signal to noise plus distortion ratio (SNDR) are achievable in simulations assuming 0.5 ps clock jitter is present. The ADC and front-end core power consumption is estimated to be 120.8 mW. The front-end is fabricated with IBM 90nm CMOS process, and a BPSK sub-Nyquist rate communication system is realized as a prototype in the testing. A 1.25 GHz reference clock with 4.13 ps jitter variance is employed in the test bench. The signal frequency,

phase and amplitude can be correctly reconstructed, and the maximum signal SNR obtained in the testing is 40 dB with single tone input and 30 dB with multi-tones test. The CS system has a better FOM than state-of-art Nyquist rate data acquisition systems taking into account the estimated PLL power.

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## CHAPTER I

### INTRODUCTION

The sampling rate of traditional analog-to-digital conversion (ADC) architectures needs to be at least twice the signal bandwidth to achieve alias free sampling [1]-[2]. The increasing demand for systems with both higher bandwidth and lower power consumption motivates the search of innovative ADCs, especially when sampling rates reach several GHz. To this end, the time-interleaving structure [3] [4] [5] [6] [7] and the multi-channel filter-bank approach [8] [9] have been proposed. However, the power consumption of these topologies is still high for many pressing applications such as wideband systems or power spectral estimation in cognitive radios [10]

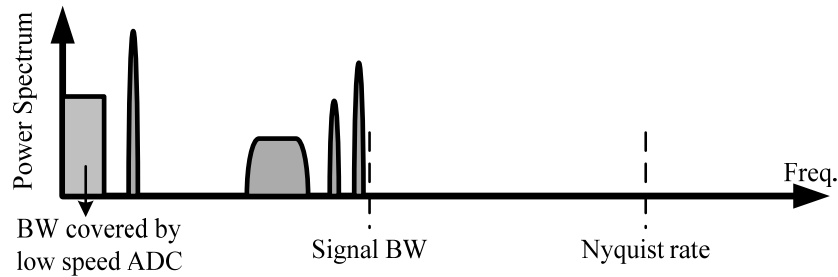


Fig. 1.1 Signals found in wireless systems are sparse in the frequency domain

[11]. Fortunately, a closer look at some of these applications reveals that the signal bandwidth is not always fully occupied simultaneously. In the particular case of wireless communications, many channels are typically unoccupied [12] which leads to a signal

that exhibits sparsity in the frequency domain as shown in Fig. 1.1. The sparsity of many real systems is a remarkable property that can also be found in several cases such as time-domain for impulse radio UWB signals [13], and the wavelet-domain for images [14].

When the signal is very sparse, the receiver can operate at a much lower frequency than the Nyquist rate [15] [16], enabling the realization of efficient signal digitizers for several transformative applications that are unrealizable with conventional receiver front-ends and data converters.

A frequency sparse signal such as the one shown in Fig.1.1 can be digitized using traditional superheterodyne radio receivers where the signal channels are selected individually for down-conversion to baseband [17]. However, in applications such as cognitive radio, it is desired to simultaneously observe the entire frequency spectrum composed of many channels, and then to isolate the signals of interest whose location is unknown a priori [10] [11]. Achieving this with multiple local oscillators and traditional down-conversion becomes cumbersome and impractical. To this end, the CS analog front-end replaces the LO mixing signal with a pseudo-random signal that emulates white noise as depicted in the architecture shown in Fig. 1.2. By mixing the input signal with a random LO signal, the signal is randomized and the information of each channel spreads over the entire bandwidth. Depending on the sparsity level, it is possible to use a low speed ADC to sample the randomized

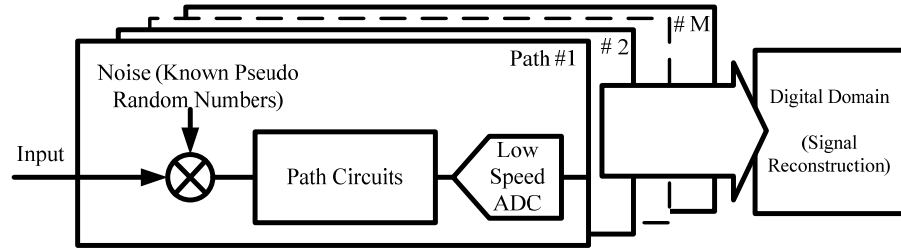


Fig. 1.2 Compressive sample parallel topology for sampling wideband signals with low speed ADCs

signal. Given these samples, several reconstruction algorithms can be used to estimate the signal information [15][16][18].

The CS front-end can be realized by circuit architectures similar to traditional receivers as presented in the following subsections. However, the impact of circuit level non-idealities is fundamentally different in CS receivers.

In this dissertation, a circuit implementation of the CS architecture is taken as an example to provide a thorough analysis of circuit noise, jitter, distortion and other impairments. The dissertation is organized as follows. Chapter II gives a brief introduction to the CS theory and the basic circuit architecture is discussed. Implementation at the circuit level is provided in Chapter III. Further analysis on the practical limitations due to jitter, noise and distortion is provided in Chapter IV and V. In Chapter VI, the detailed design specifications and simulation results employing a conventional 90nm CMOS technology are included. Chapter VII presents the testing results of a CS system implemented with discrete components and the CS front-end fabricated with the 90 nm CMOS process, with the conclusions provided in the last Chapter.

## CHAPTER II

### CS THEORY AND THE BASIC CIRCUIT ARCHITECTURE

In this Chapter, as an example to introduce the basic concepts of the CS theory, the input signal is assumed to be sparse in the frequency domain. Let the input signal be represented by a vector  $x \in \mathbb{R}^{N \times 1}$ . Define  $y \in \mathbb{R}^{N \times 1}$  as the spectrum of the original signal  $x$ , and we have  $y = \psi x$ , where  $\psi \in \mathbb{C}^{N \times N}$  is the  $N$ -point Fourier transform matrix. Since  $x$  is sparse in the frequency domain, there are only  $K$  significant elements in  $y$ , with  $K < N$ . The other  $N-K$  elements have very small contribution to the signal and can be ignored. When the other  $N-K$  elements are set to “0”, we can still almost perfectly reconstruct the input signal via  $x = \psi^H y$ , which means that the original input  $x$  is compressed into an effectively shorter vector  $y$ . Due to the sparsity,  $y$  is able to fully capture the information contained in  $x$  (Fig. 2.1).

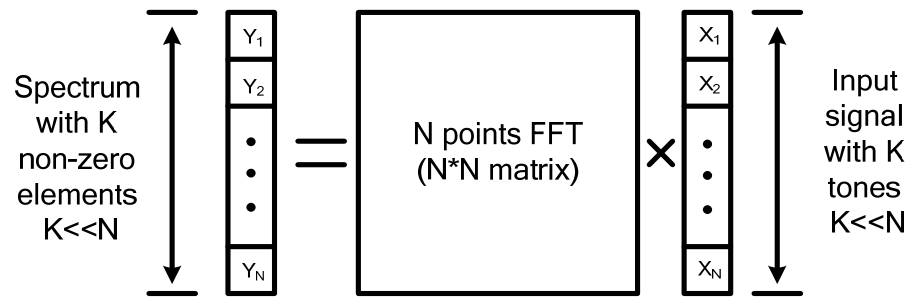


Fig. 2.1 An example of signal compression

A matrix transform such as the FFT is usually done in the digital domain and the ADC still needs to work at high frequency to fully sample  $x$  before the compression. However,



a CS receiver front-end can condition  $x$  before the sampling so that the ADC can work at lower speed. The original input  $x$  can be reconstructed with high probability by sampling only  $M$  linear random projections of  $x$ :  $s = \Phi x$ , where  $\Phi \in R^{M \times N}$ ,  $s \in R^{M \times 1}$  and  $M \ll N$ . The matrix  $\Phi$  is a known realization of a random process. In this work, random binary elements (+1/-1) are employed because they are readily generated using simple high bandwidth circuitry. Since  $y = \psi x$  and  $s = \Phi x$ , we have  $\Phi \psi^H y = s$ . The vector  $y$  is shorter than  $s$ , so there exist many solutions for  $y$  that satisfy this condition. According to CS theory, if  $x$  is a sparse signal over  $\psi$ , the  $y$  with minimum number of non-zero elements is the solution that correctly represents  $x$ . In other words,  $y$  can be solved via the optimization problem given by,

$$y = \arg \min \|y\|_1, \text{ s.t. } \Phi \psi^H y = s.$$

The original signal can be reconstructed when  $y$  is solved through  $x = \psi^H y$ . Algorithms for solving this optimization problem are discussed in classical CS literature [15][16][18]. The reconstruction complexity depends on the specific reconstruction algorithm. For example, the computational complexity is  $\Omega(S^3)$  when LP is used for signal reconstruction; whereas the computational complexity is  $\Omega(SK^2)$  for the OMP algorithm [18]. The number of measurements  $M$  only needs to be greater than  $K \log_2(N/K)$  to ensure that the sampled information is sufficient with high probability. An example of OMP reconstruction algorithm is included in Appendix A. The CS theory

is only applicable when the signal is sparse. Note that the signal reconstruction complexity is higher than the FFT, although there are many ongoing efforts to bring the complexity down to that of the FFT ( $N \log N$ ).

The sampled vector  $s$  can be generated by the circuit architecture in Fig. 2.2. The signal is fed into the parallel paths, and each path is associated with an independent pseudo-random number (PN) binary sequence. These PN sequences form the rows of the matrix  $\Phi$ . The integration results in the inner product of  $x$  and the PN sequence, each of which is an element of  $s$ . Then,  $s$  is sampled and processed in the digital domain for signal reconstruction. The continuous analog input signal is represented as a discrete time vector  $x$  whose data rate equals the PN sequence. This representation is alias-free only if the data rate of the PN sequence is higher than twice the bandwidth of the analog input. Thus the speed of the PN generator circuit needs to be as high as the Nyquist rate.

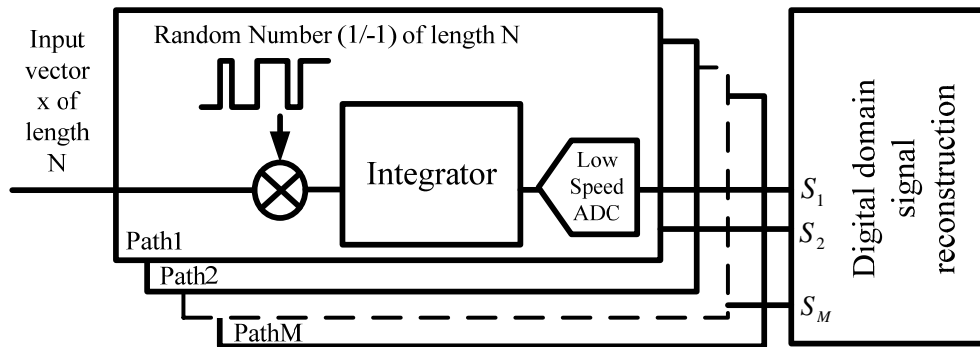


Fig. 2.2 Parallel circuit implementation of traditional compressed sensing

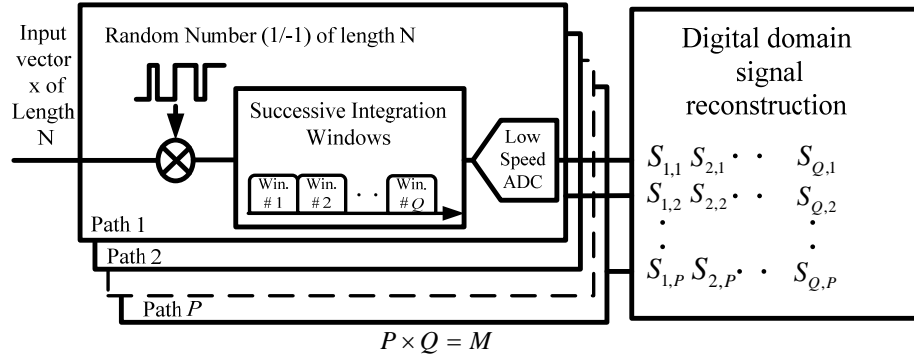


Fig. 2.3 Parallel segmented compressed sensing

Fig. 2.2 illustrates the idea of traditional CS, where each parallel path generates one sample during one signal period. From the implementation perspective, this is unrealistic because of the necessity of many parallel paths. Therefore, we use segmentation, i.e. windowing, to reduce the number of parallel paths, and each path generates multiple samples each of which is a random projection of one segment of the signal, as illustrated in Fig. 2.3 [19]. In this proposed Parallel Segmented CS (PSCS) architecture, the randomized signal after the mixer is equally divided into  $Q$  segments in the time domain. Each path integrates  $Q$  segments of the randomized signal, yielding  $Q$  samples in each path. Reference [19] shows that the required number of overall samples remains the same as compared to Fig.2.2, and thus the required number of paths in Fig.2.3 is  $P=M/Q$ . The signal reconstruction is performed digitally using the sampled matrix  $S$  (Fig.2.3). The math representation of the optimization problem for PSCS is given in Appendix B.

The reconstructed signal quality is simulated and plotted in Fig. 2.4. Suppose the input signal contains 256 sub-carriers and the bandwidth is around 1.5 GHz. The locations of  $K$  active sub-carriers are chosen randomly. The signal sparsity representing

the spectral occupancy is defined as  $K/256$ . In the simulation, all active sub-carriers have the same amplitude and 1000 iterations are run for each sparsity setup. The signal quality is represented by its signal to noise ratio (SNR). The CS system sampling rate is defined as  $SR_{path}P$ , where  $SR_{path}$  is the sampling rate of each single path and  $P$  is the number of paths.

Fig. 2.4 shows that the required sampling rate for a given SNR depends on the signal sparsity. For example, when there are 10 active tones in the signal bandwidth (4% sparsity and spectral occupancy), the required system sampling rate to achieve perfect signal quality ( $SNR > 100$  dB) is as low as 26% of the Nyquist rate, or roughly 800 MHz. Based on Fig. 2.4 we propose a PSCS receiver that detects wideband signals over 10 MHz ~ 1.5 GHz bandwidth as an example in following Chapters. For illustration, the input signal is assumed frequency domain sparse. Also it is assumed that the input signal sparsity is 10/256 with which the system sampling can be significantly lowered, but it needs to be emphasized that the approach is flexible and the system is adaptable to varying levels of sparsity.

The system incorporates 8 parallel paths whose outputs are sampled at 110 MHz. The input signal power is assumed to be -20 dBm referred to 50 ohm.

In reality the reconstructed SNR is limited by many circuit non-idealities such as clock jitter, thermal and flicker noise, distortion and the quantization noise of ADCs. In the following Chapters it is shown that the impact of the non-idealities is different from that in traditional receivers due to the signal randomization. The reconstructed SNR of the proposed system is targeted at 44 dB (7 bits) in simulations. The error energy

individually induced by jitter, circuit noise, distortion and the quantization noise is designed to be less than -50 dB as referred to the signal power in order to achieve an overall SNDR of 44 dB.

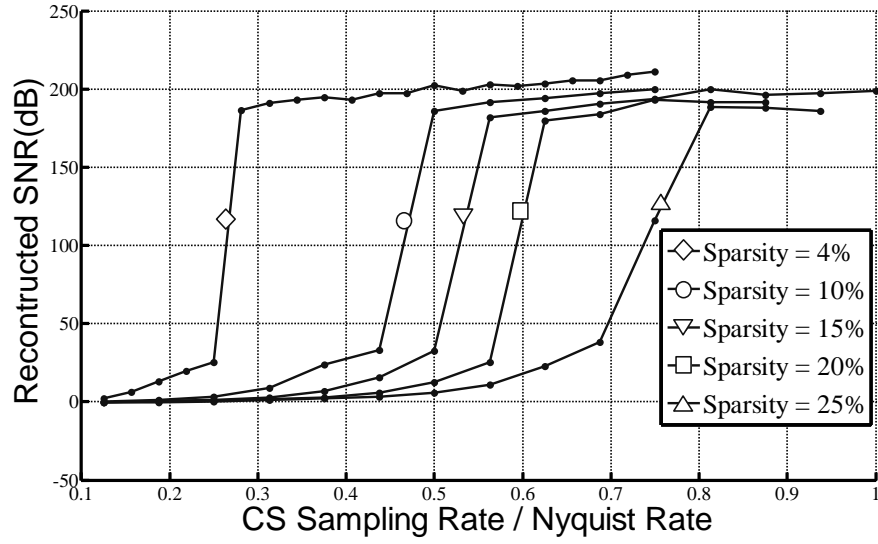


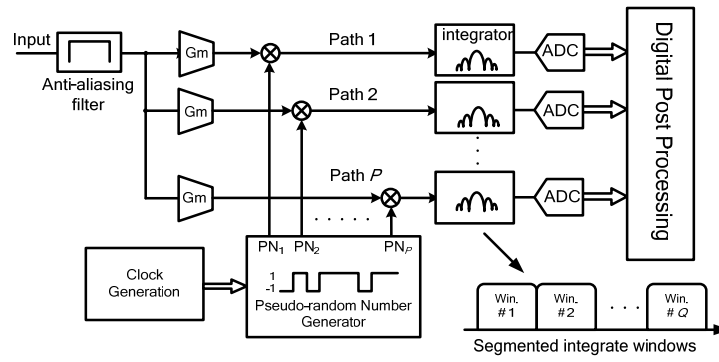
Fig. 2.4 Reconstructed Signal *SNDR* vs. signal sparsity & sampling rate

## CHAPTER III

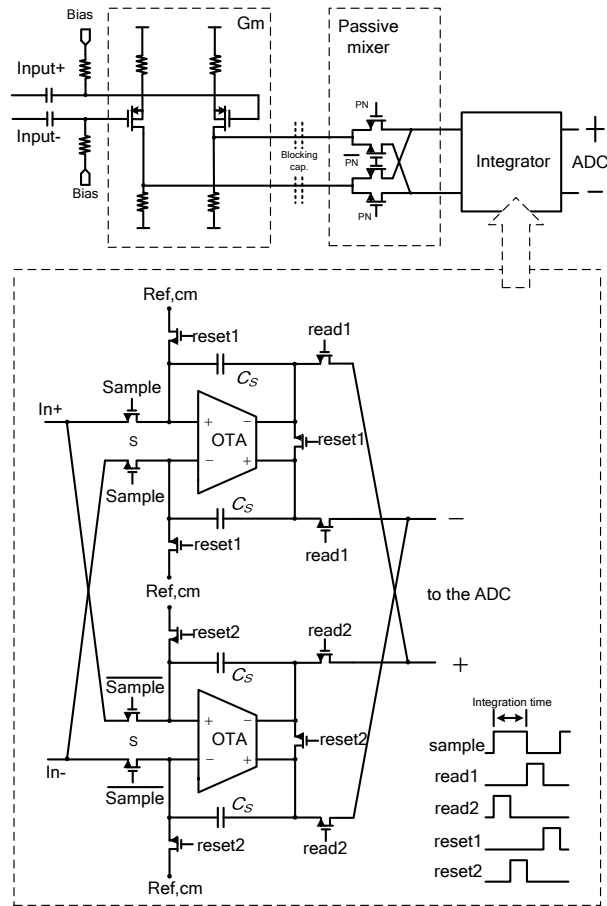
### CIRCUIT LEVEL IMPLEMENTATION

#### 3.1 The PSCS front-end circuit architecture

A current mode parallel-path front-end is suitable because current mode architectures have the benefit of allowing convenient design of mixers and reconfigurable integrators. The applicable front-end is shown in Fig. 3.1. An example of PN generator can be found in [20]. It is assumed that an out-of-chip high-order anti-aliasing filter is present at the input of the receiver and selects the signal bandwidth 10 MHz ~1.5 GHz. The input voltage is converted into signal current through the transconductance stages  $G_m$ . The signal current is then mixed with the PN binary sequences (1 or -1) from the PN generator. The mixer output current is integrated over segmented integration windows. The integrators' outputs are then digitized and post-processed digitally. The integrator consists of two time-interleaved branches that provide successive integration windows. A simplified schematic of the integrator is shown in Fig.3.2. The capacitors are first reset, and then the mixer output current is injected into one of the capacitors  $C_S$  during the integration time  $T_i$ . After that the charge is transfer to the ADC. The integrator also serves as the sample and hold (S&H) circuit before the ADC. The sampling rate is reconfigurable, depending on the frequency of the controlling clocking scheme and is set according to the signal sparsity. It can also operate up to Nyquist rate if the signal does not exhibit enough sparsity to be processed using the CS theory.



(a)



(b)

Fig. 3.1 a) Circuit implementation of the proposed CS receiver

b) Detailed circuitry of one path

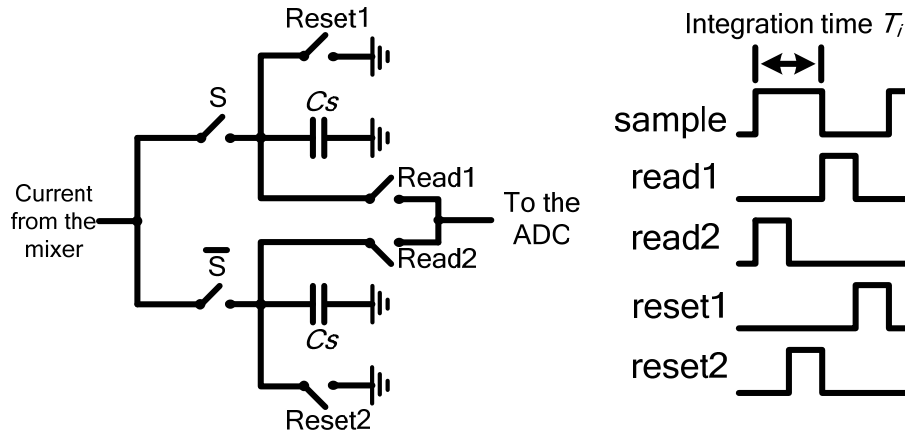


Fig. 3.2 Simplified two branch passive integrator

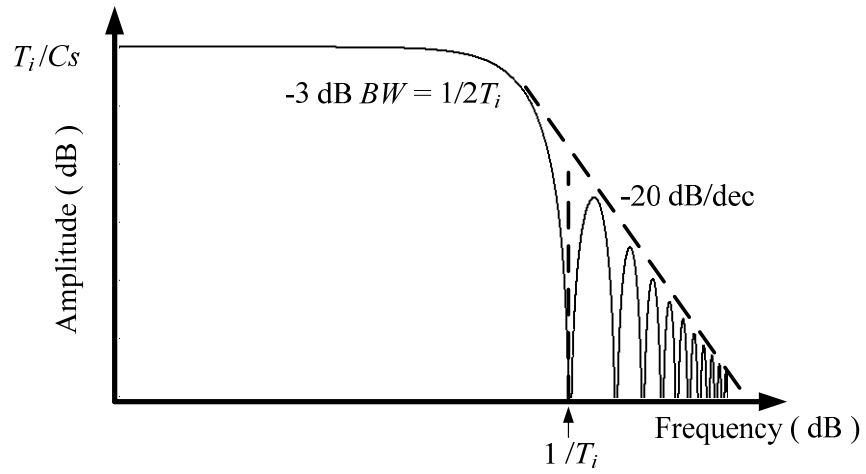


Fig. 3.3 Frequency response of the windowed integrator

The final realization of the integrator in Fig.3.1b incorporates two operational transconductance amplifiers (OTAs) to optimize the operation of the mixers by limiting the switches signal swing due to the low impedance provided by the closed loop operation of the OTA. The sinc type frequency response of the windowed integrator is



shown in Fig.3.3, where  $T_i$  is the duration of a single segmented integration time window. The -3 dB bandwidth of the transfer function is  $1/2T_i$ , which is also controlled by the clock frequency.

### 3.2 Parallel path ADCs

Each path employs a low speed ADC that samples the randomized signal at the output of the integrator. The sampling rate is around 110 MS/s and the effective number of bits (ENOB) of the ADC needs to be 8 bits to achieve 50 dB SNR. Pipeline ADCs or SAR ADCs can meet this specification with low power consumption. In [21], a pipeline ADC achieves 7.9 ENOB and 50 MS/s with power consumption of 1.44 mW. In [22], a SAR ADC achieves 8.53 ENOB and 100 MS/s sampling rate with power consumption of 1.46 mW. Performance, non-idealities, and the design procedure of traditional Nyquist ADCs have been extensively discussed in existing literatures. Rather than designing an ADC, the published state of art ADCs were drawn on to realistically estimate the power consumption of the system with ADCs incorporated. The achievable signal to noise plus distortion ratio (SNDR), power consumption and sampling rate of relevant ADCs published in ISSCC08 and 09 are shown in Fig.3.4. According to the technology trend [23], a 110 MHz / 8 ENOB ADC consumes approximately 3.5 mW power. It is then expected that the 8 ADCs should consume an overall power around 28 mW.

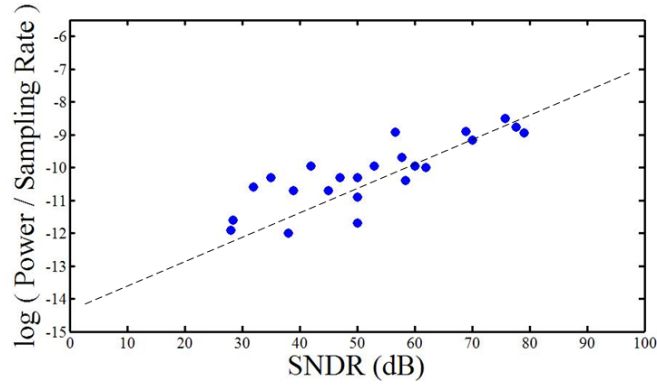


Fig. 3.4 Performance of State-of-art ADCs reported in ISSCC-08-09

### 3.3 Front-end signal gain

We begin the analysis by calculating the signal gain of the front-end as,

$$|Gain_s|^2 = \frac{V_{sig,output}^2}{V_{sig,input}^2}. \quad (3.1)$$

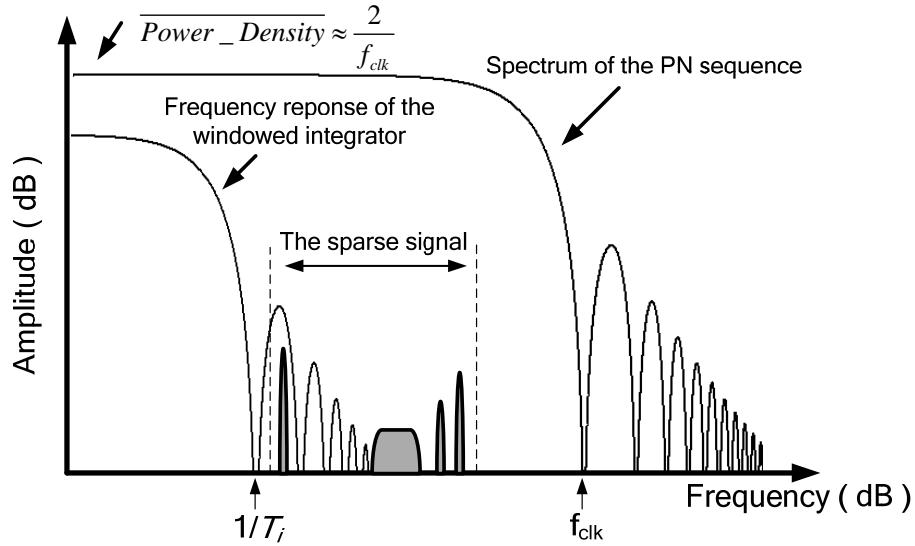


Fig. 3.5 The transfer function of the integrator, the spectrum of the PN sequence and the spectrum of the sparse input signal

Here  $V_{sig,input}^2$  is the total signal power present at the receiver input and  $V_{sig,output}^2$  is the total signal power at the output of one integrator.

The transfer function of the integrator, the sinc type spectrum of the PN sequence and the typical signal spectrum are shown in Fig. 3.5. The transfer function of the windowed discrete time integrator can be found as,

$$H_i(f) = \frac{T_i}{C_s} \text{Sinc}(\pi f T_i). \quad (3.2)$$

The power spectrum of the PN sequence is given by,

$$\overline{PN^2(f)} \approx \frac{2}{f_{clk}} \left| \text{Sinc}\left(\frac{\pi f}{f_{clk}}\right) \right|^2. \quad (3.3)$$

The spectrum of the PN sequence rolls off at high frequency, so the signal tones at higher frequencies contribute less power to the randomized signal. By combining Eqns. (3.1)-(3.3), the front-end signal gain is given by,

$$|Gain_s|^2 = \frac{\int_0^\infty \left[ V_{sig,input}^2(f) Gm^2 \right] * \overline{PN^2(f)} |H_i(f)|^2 df}{\int_{10MHz}^{1.5GHz} V_{sig,input}^2(f) df}. \quad (3.4)$$

Where the symbol \* stands for convolution. Notice that the front-end gain is frequency dependent. Since the locations of the input signal tones are random, it is not possible to predict a fixed gain. However some practical cases can be considered. When the input tones are concentrated at very low frequencies, the front-end yields a maximum gain given by,

$$|Gain_s|_{MAX}^2 = \left( \frac{1}{C_s} \right)^2 T_i \frac{|Gm|^2}{f_{clk}}. \quad (3.5)$$

On the other hand, when the input signal power is at the upper edge of the signal bandwidth, which is  $f_{clk}/2$ , the front-end power gain is degraded by  $|Sinc(\pi/2)|^2$  and yields a minimum gain given by,

$$|Gain_s|_{MIN}^2 = 0.4 \left( \frac{1}{C_s} \right)^2 T_i \frac{|Gm|^2}{f_{clk}}. \quad (3.6)$$

Additionally, when the signal tones are normally distributed over the entire signal bandwidth, the signal gain can be approximated as,

$$|Gain_s|_{Normal}^2 = 0.67 \left( \frac{1}{C_s} \right)^2 T_i \frac{|Gm|^2}{f_{clk}}. \quad (3.7)$$

Therefore, in general the signal gain can be expressed as,

$$|Gain_s|^2 = \lambda \left( \frac{1}{C_s} \right)^2 T_i \frac{|Gm|^2}{f_{clk}}, \quad (3.8)$$

where  $\lambda$  is a factor varying between 0.4 and 1.  $\lambda$  is determined by the spectral distribution of the input signal; e.g. with a single tone input  $\lambda = |Sinc(\pi f_{signal} / f_{clk})|^2$  and with a normally distributed multi-tone input the value of  $\lambda$  is around 0.67.

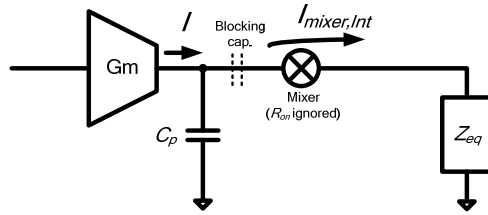


Fig. 3.6 Signal current splits between parasitic and the active integrator

### 3.4 Front-end bandwidth

As depicted in Fig.3.6, at the output of the Gm stage the blocking capacitor introduces significant parasitic capacitance to ground. The switches in the mixer also contribute with additional parasitic capacitance at this node.  $C_p$  takes away part of the signal current and limits the system bandwidth. The receiver bandwidth depends on  $C_p$  and the input impedance of the active integrator  $Z_{eq}$ .

Detailed analysis shows that  $Z_{eq}$  varies with different OTA structures. For instance, let's consider the two stage OTA [24] shown in Fig. 3.7 (a); the simplified single-ended model for the active integrator is shown in Fig. 3.7 (b). At high frequency  $C_S$  and  $C_C$  can be considered as AC short circuits, then  $Z_{eq}$  can be approximated as,

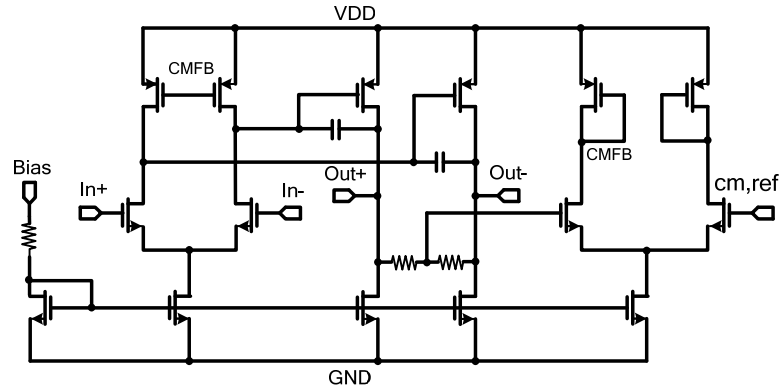
$$Z_{eq} \approx \frac{1}{-gm_1} // \frac{1}{gm_2} // \frac{1}{s(C_{o1} + C_L)}. \quad (3.9)$$

When the active integrator is sampling the input current, the 'read' switches in Fig.3.1 are OFF and the ADC is not loading the OTA. In this case,  $C_{o1} + C_L$  in Fig.3.7 (b) is small compared with  $C_p$  in Fig.3.6, leading to,

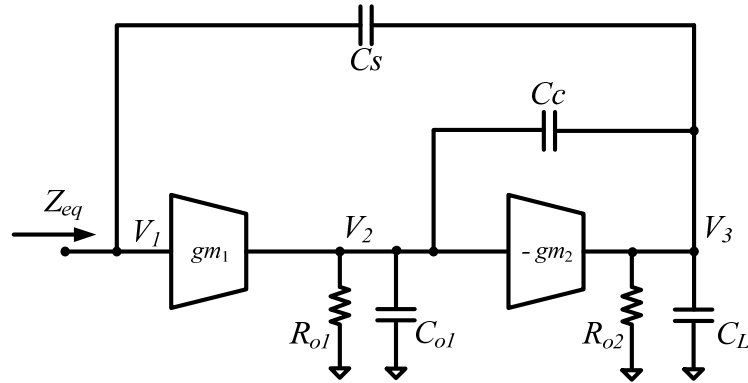
$$Z_{eq} \approx \frac{1}{gm_2 - gm_1}. \quad (3.10)$$

The bandwidth of the signal current path that feeds the mixers and integrators is given by,

$$BW_{path} \approx \frac{gm_2 - gm_1}{2\pi C_p}. \quad (3.11)$$



(a)



(b)

Fig. 3.7 a) A typical two stage Miller compensation OTA

b) simplified active integrator model

Therefore, enough power at the second stage must be used to increase  $gm_2$ . This usually leads to over-designing the second stage of the OTA. In this case, the OTA can achieve enough phase margin without the compensation resistor in series with  $C_C$ , hence the compensation resistor is removed to lower noise. e.g., with  $C_p = 300$  fF and  $BW = 1.5$  GHz,  $gm_2$  needs to be 3 mS larger than  $gm_1$ .

### 3.5 The PN generator

In a Compressive Sensing receiver, the requirements on the analog circuit blocks are significantly relaxed. The baseband filter and the ADC work at low frequency. However, the speed of the PN sequence needs to be at least equal to the Nyquist rate so the PN generator still needs to work at high speed. The maximum input bandwidth that the receiver can process depends on how fast the PN generator is. The design bottle neck is moved from analog parts to digital clock generating blocks such as the PN generator.

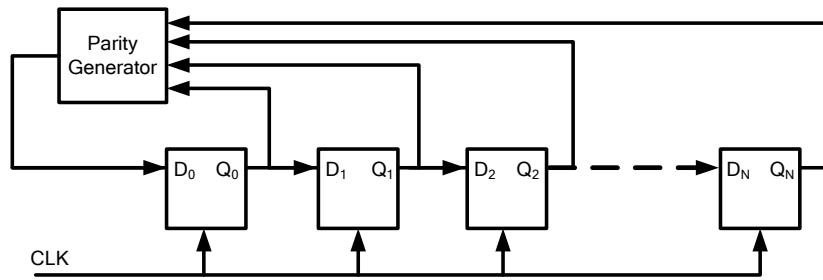


Fig.3.8 A traditional PN generator

A typical PN generator formed by a flip-flops pipeline is shown in Fig.3.8. The outputs of the flip-flops are fed back to the first one through a parity generator, which yields output of '1' if an odd number of its inputs are at logic '1' and yields '0' if an even number of its inputs are at logic '1'. The generated PN sequence only maintains the randomness within finite lengths and it will repeat itself when the PN generator keeps running at the end of the finite length of pseudo-random sequences. With different number of flip-flops, different specific parity generators are required to yield the maximum achievable length. Denote  $N$  as the number of the employed flip-flops, the maximum achievable

PN length is  $2^N - 1$ . It is preferred to choose a parity generator with minimum number of inputs in order to minimize its delay. For example, when 11 flip-flops are used, the optimum parity generator is simply a XOR gate, fed by the outputs of the 8th and the 11th flip-flops. Assume a single flip-flop is composed of two D-latches as shown in Fig.3.9,

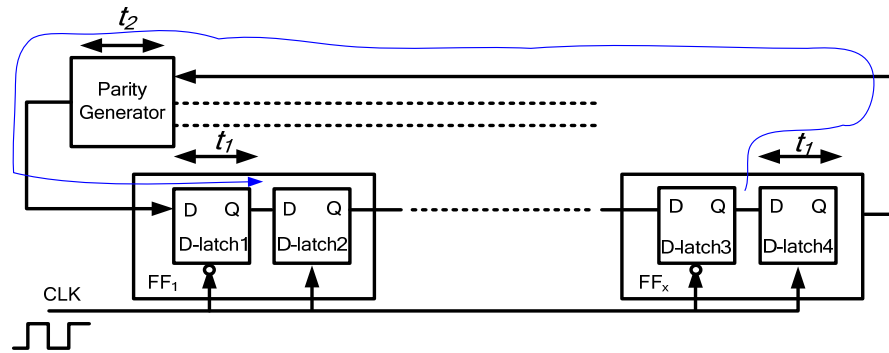


Fig.3.9 Signal delay in the PN generator

The first D-latch keeps its state when CLK is '1' while the latter one keeps its state when CLK is '0', then the flip-flops are triggered at the rising edge of the master CLK. The most critical signal delay in the feedback loop is from one of those flip-flops that feed the parity generator to the first flip-flop. Denote the delay of a D-latch as  $t_1$ , and the delay of the XOR gate as  $t_2$ . Before the rising edge of CLK, the output of D-latch3 has settled to the output of the previous flip-flop. After the rising edge of the CLK, it takes  $2t_1 + t_2$  for D-latch1 to settle. Note that the next rising edge of CLK needs to come later than D-latch1 settles in order to ensure a well-defined logic state, then the minimum period of the master CLK is  $2t_1 + t_2$ , and the maximum speed of the PN generator is  $1/(2t_1 + t_2)$ . With the IBM 90nm CMOS technology  $t_1$  and  $t_2$  are around 100 ps. The



conservative maximum speed of the PN generator is around 3 GHz. In this case, the maximum allowed input signal bandwidth of the Compressive Sensing front-end is 1.5 GHz. We may push the PN generator to work at higher speed such as 4 GHz by carefully designing the layout.

For going to higher signal bandwidth, new PN generator architectures need to be explored. Sometimes the parity generator has multiple inputs and its high complexity makes  $t_2$  dominate. In order to relax the delay requirement of the parity generator, the two D-latches in the first flip-flop may be exchanged to make it be triggered at the falling edges of CLK (Fig.3.10). The triggering moment of D-latch2 comes half a period later so the minimum period of CLK is  $(2t_1+t_2)/1.5$ . However, after the falling edge of CLK, the first D-latch of the second flip-flop needs to settle before the following rising edge of CLK, so the minimum period of CLK needs to be longer than  $4 t_1$ . The maximum speed of the PN generator is  $1/ \max [(2t_1+t_2)/1.5, 4 t_1]$ . The architecture in Fig.3.10 may boost the speed of PN when  $t_2$  is significantly longer than  $t_1$ .

Furthermore, high speed PN sequence may be generated by combining multiple parallel PN generators. As shown in Fig.3.11, a parity generator may be employed to

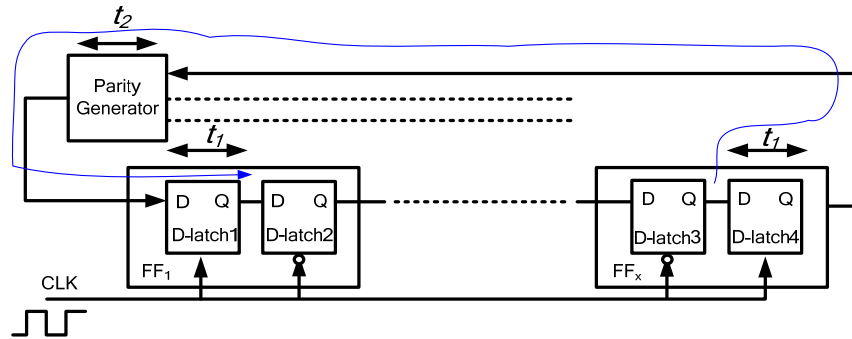


Fig.3.10 Signal delay in the modified PN generator

combine outputs of several PN generators. The CLKs of those PN generators are at the same speed but different phases. Assume there are  $M$  PN generators, the phase of the  $n$ th CLK is  $2\pi n / M$ .

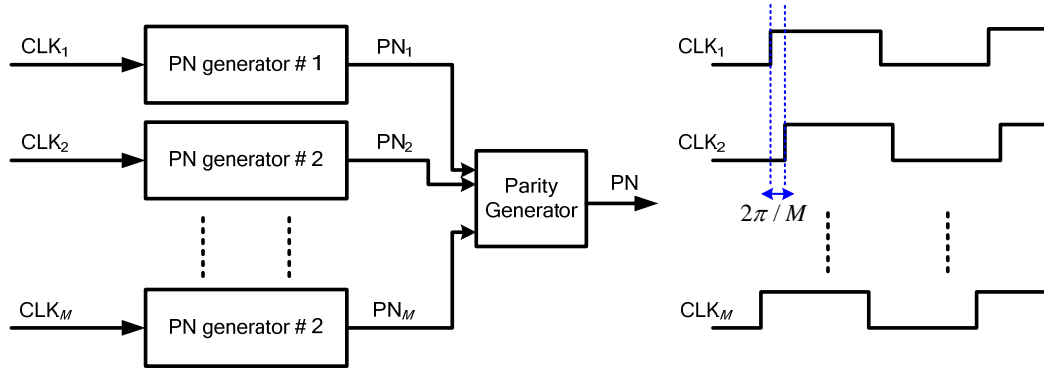


Fig.3.11 Parallel PN generation

Ideally the speed of the final generated PN sequence is boosted by  $M$  times. However, note that the speed of this PN sequence is still limited by the delay of the parity generator and the complexity and delay of the parity generator increase when it has more inputs. It is impossible to stack infinite number of PN generators to get an extremely high speed PN.

The length of the final generated PN sequence is  $MQ$  where  $Q$  is the length of the low speed PN sequence generated by each single PN generator. To maintain the randomness of the final PN sequence, those  $M$  low speed PN sequences need to be uncorrelated. In order to achieve this, each single PN generator needs to be capable of generating a PN sequence of length  $MQ$ . Those PN generators are reset to different initial states so that the PN sequence of length  $MQ$  is equally divided into  $M$  uncorrelated pieces, each of which is generated by a single PN sequence generator.

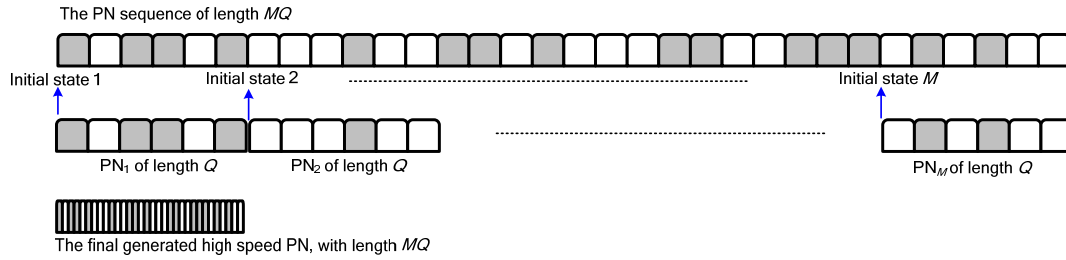


Fig.3.12 Illustration of the high speed PN generation

The final PN sequence is generated by combining those  $M$  un-correlated low speed PN sequences (Fig.3.12). For example, assume two individual PN generators are combined to generate a high speed PN sequence of length 2047, each PN generator needs to contain 11 flip-flops. Both of them can generate a PN sequence of length 2047. One of them starts at the very beginning of the PN sequence while the other starts with the 1024<sup>th</sup> number. The parity generator is a XOR gate, combining the two un-correlated PN sequence. Assume the two PN generators run at 4 GHz, the period of the CLK signals is 250ps. The CLK of the second PN generator lags 125ps. The data rate of the final PN sequence is 8 GHz. An example of a 8 GHz PN sequence simulated with SPICE is shown in Fig.3.13.

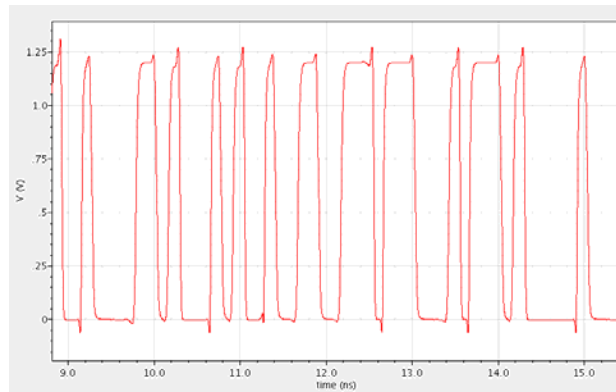


Fig.3.13 A 8 GHz high speed PN sequence

Each individual PN generator only affects the final output when it flips, and only one PN generator is flipping at the same time, so the jitter variance at the transition of the final high speed PN sequence is expected to be the same with each single PN sequence.

## CHAPTER IV

### CLOCKING JITTER

#### 4.1 Overall jitter impact to the CS receiver

Jitter in the PN sequences and the sampling clocks limit the achievable SNR. The noise introduced by jitter in the PN sequences may dominate the SNR performance since the speed of the PN sequences is much higher than the sampling clock frequency. Thus, only the PN jitter is considered in the following analysis whereas the sampling clock jitter is ignored. The jitter in the PN sequences introduces some pulse errors, as shown in Fig.4.1. The width of each pulse is equivalent to the timing jitter at that switching instant, which randomly changes according to the jitter distribution. Denoting the real PN sequence and the ideal sequence as  $PN_r$  and  $PN_i$ , respectively, then,

$$PN_r = PN_i + e(t), \quad (4.1)$$

where  $e(t)$  is the jitter error, which can be assumed uncorrelated with  $PN_i$ . The typical spectra of  $PN_i$  and  $e(t)$  are plotted in Fig. 4.2. Denoting  $N_j^2$  as the jitter induced noise power at the output of the integrator, it follows that

$$N_j^2 = \int_0^\infty \left| \left[ \left( V_{sig,input}(f) Gm \right) * E(f) \right] H_i(f) \right|^2 df, \quad (4.2)$$

where  $E(f)$  and  $V_{sig,input}(f)$  are the power spectrum of  $e(t)$  and the input signal.  $H_i(f)$  is the transfer function of the integrator.  $e(t)$  is composed of a train of randomly spaced out narrow impulses. Then the spectrum  $E(f)$  is rather flat throughout the bandwidth of

$V_{sig,input}(f)$  and  $H_i(f)$ . Therefore  $E(f)$  can be approximated as thermal noise, whose variance is determined by the voltage controlled oscillator and buffer noise components present in the PN block. The power spectral density of  $e(t)$  shows that the density of  $E(f)$  in the bandwidth of interest is given by  $4\sigma_j^2 f_{clk}/\text{Hz}$ , where  $\sigma_j$  is the jitter standard deviation (also known as the jitter root-mean-squared (rms) value). The density of  $E(f)$  is derived in section 4.2. Substituting into equation (4.2) and using (3.2), it can be found that,

$$N_j^2 = 2 \left( \frac{1}{C_s} \right)^2 T_i \sigma_j^2 f_{clk} V_{sig,input}^2 |Gm|^2. \quad (4.3)$$

According to equation (3.8), the power of the ideal signal output with an ideal PN sequence is given by,

$$V_{sig,output}^2 = \lambda \left( \frac{1}{C_s} \right)^2 T_i \frac{|Gm|^2}{f_{clk}} V_{sig,input}^2. \quad (4.4)$$

The jitter-limited SNR, denoted as  $\text{SNR}_j$  can be obtained with the help of (4.3) and (4.4) as follows,

$$\text{SNR}_j = \frac{V_{sig,output}^2}{N_j^2} = \frac{\lambda}{2\sigma_j^2 f_{clk}^2}. \quad (4.5)$$

$\lambda$  varies with different spectrum distribution of the input signal. Assuming that the input signal's spectrum is normally distributed then  $\lambda$  is approximately 0.67 leading to,

$$\text{SNR}_j = \frac{0.335}{\sigma_j^2 f_{clk}^2} \quad (4.6)$$

For example, for  $f_{clk} = 3$  GHz,  $SNR_j$  is limited to 36 dB by 3 ps<sub>rms</sub> jitter and 52 dB by 0.5 ps<sub>rms</sub> of jitter standard deviation.

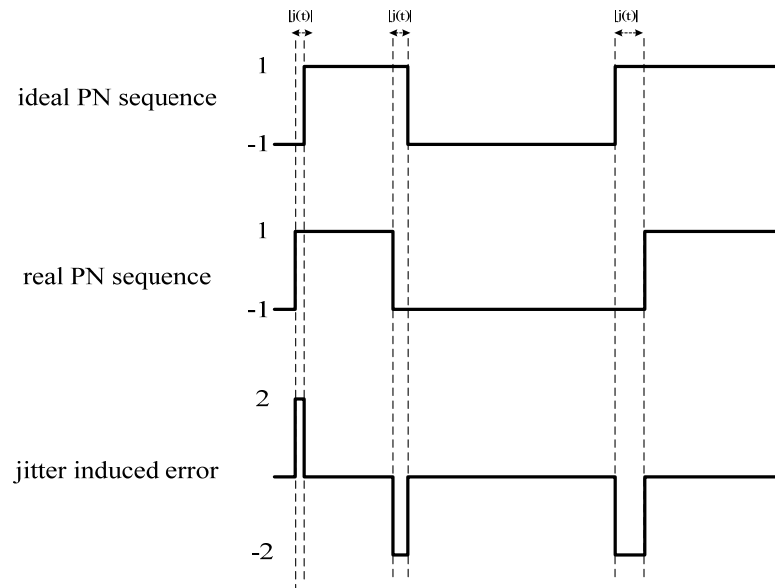


Fig. 4.1 The ideal and real PN sequences with jitter included

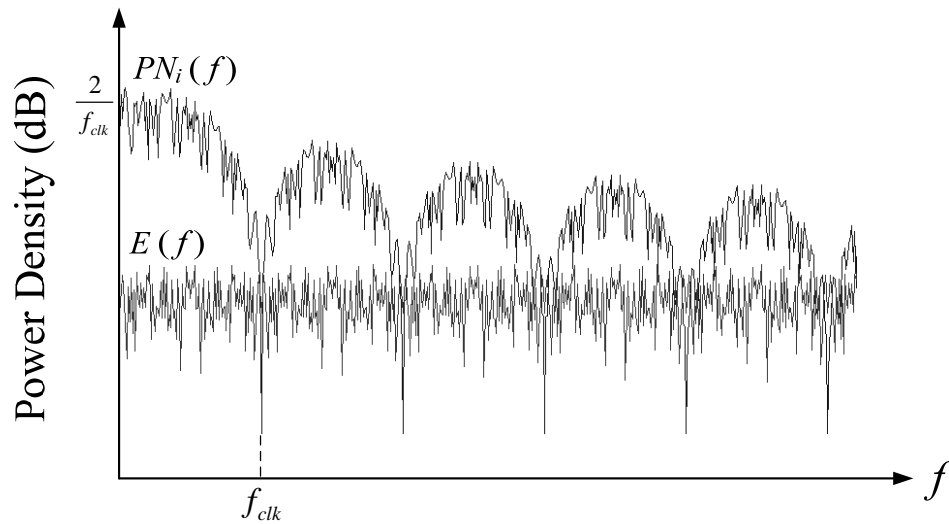
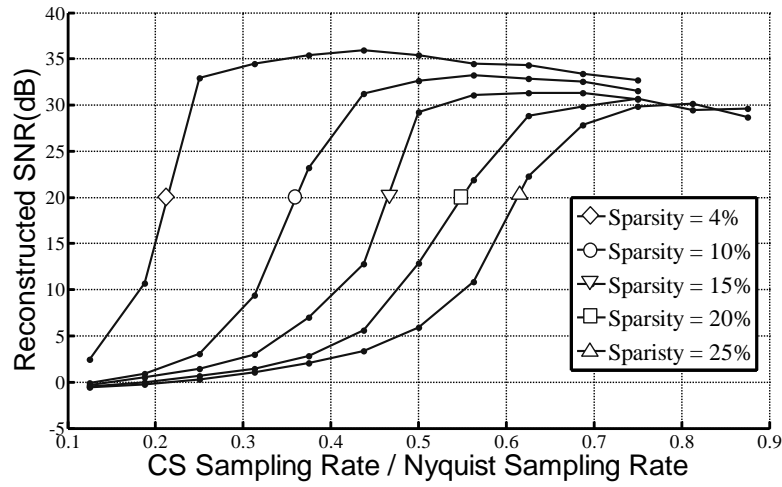
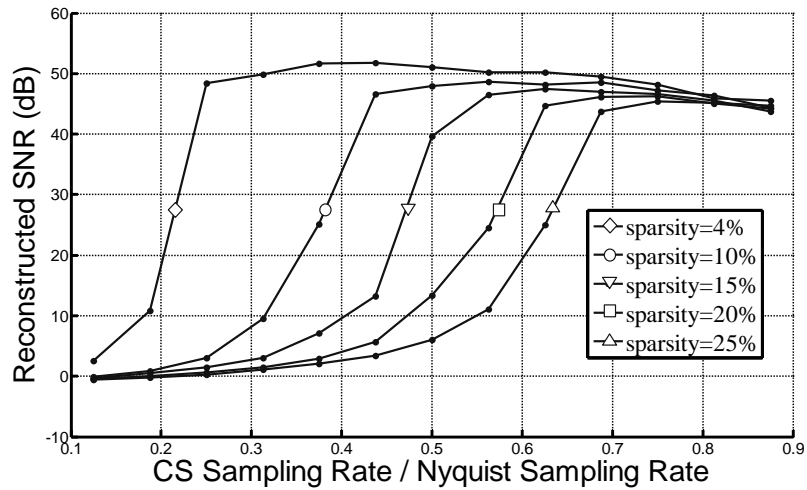


Fig. 4.2 Spectrums of the PN sequence and the jitter induced PN error  $E(f)$



(a)



(b)

Fig. 4.3 Reconstructed Signal  $SNDR$  vs. signal sparsity & sampling rate with presence of

(a)  $3 \text{ ps}_{\text{rms}}$  jitter and (b)  $0.5 \text{ ps}_{\text{rms}}$  jitter

The reconstructed SNRs with  $3 \text{ ps}_{\text{rms}}$  and  $0.5 \text{ ps}_{\text{rms}}$  of jitter were simulated at the system level and plotted in Fig. 4.3. State of the art clock generators have achieved clock



signals with  $0.2 \text{ ps}_{\text{rms}}$  jitter; e.g. [25]. In the simulations presented in Chapter VI, the jitter level was assumed  $0.5 \text{ ps}_{\text{rms}}$ .

#### 4.2 Spectrum density of $E(f)$

In section 4.1 it states that the density of  $E(f)$  in the bandwidth of interest is given by  $4\sigma_j^2 f_{clk}/\text{Hz}$ . This conclusion is derived in this section.

PN jitter induced error  $e$  is not a periodic function so it needs to be tested in a time window much longer than the clock period to estimate its spectrum distribution. As shown in Fig. 4.4, we consider  $e$  over time duration  $T$ , and  $T \gg 1/f_{clk}$ , where  $f_{clk}$  is the clock frequency of the PN generator and  $1/f_{clk}$  is the minimum possible spacing between two adjacent error impulses. A single error impulse is shown in Fig. 4.5 and its spectrum is estimated as follows.

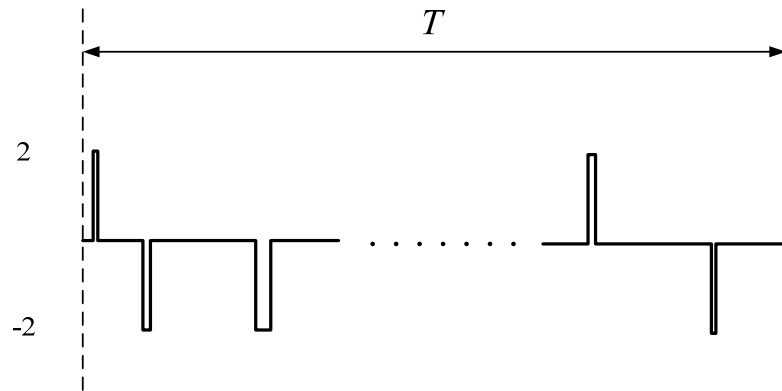


Fig.4.4 The PN error function

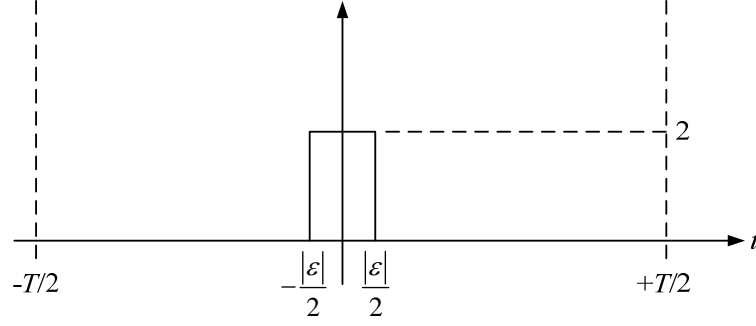


Fig.4.5 A single error impulse

Define the centre of the single impulse as the origin. For simplicity assume the magnitude of this impulse is positive. The single error impulse can be represented by,

$$i(t) = 2, \text{ for } -\frac{|\varepsilon|}{2} < t < \frac{|\varepsilon|}{2} \quad (4.7)$$

$$i(t) = 0, \text{ otherwise} \quad (4.8)$$

The fourier series of  $i(t)$  is given by,

$$a_0 = \frac{1}{T} \int_{-T/2}^{T/2} i(t) dt = \frac{2|\varepsilon|}{T} \quad (4.9)$$

$$a_n = \frac{2}{T} \int_{-T/2}^{T/2} i(t) \cos(2\pi n t / T) dt = \frac{4}{\pi n} \sin\left(\frac{\pi n |\varepsilon|}{T}\right) \quad (4.10)$$

When we only consider the power density at low frequencies,  $\frac{\pi n |\varepsilon|}{T} \ll 1$ , we have,

$$a_n = \frac{4|\varepsilon|}{T} \quad (4.11)$$

The power density at low frequency is given by,

$$P = \frac{a_n^2}{2} \frac{1}{\Delta f} \quad (4.12)$$

Where  $\Delta f$  is the frequency spacing between  $\cos(2\pi nt/T)$  and  $\cos[2\pi(n+1)t/T]$ , which is equal to  $1/T$ . We have,

$$P = 8|\varepsilon|^2 / T \quad (4.13)$$

Within the time window  $T$ , the PN sequence contains  $f_{clk}T$  random binary numbers, error impulse only occurs when the binary number switches. The possibility of switching at the end of random binary numbers is 50%. Approximately the PN switches  $f_{clk}T/2$  times so there exist  $f_{clk}T/2$  error impulses. They are uncorrelated and their low frequency power density adds up. The overall low frequency power density of the PN sequence is give by,

$$P_{PN} = \left(8|\varepsilon|_{mean}^2 / T\right) (f_{clk}T / 2) = 4\sigma_j^2 f_{clk} \quad (4.14)$$

where  $\sigma_j^2$  is the jitter variance.

## CHAPTER V

### NOISE AND DISTORTION

#### 5.1 Noise analysis

In conventional receivers, the in-channel noise is a major concern. However, in a CS receiver, the signal is randomized such that the signal spectrum spreads out and overlaps with the noise present over the entire bandwidth. The noise in a single channel cannot be isolated and the total integrated noise over the signal bandwidth needs to be considered to estimate the SNR. In the rest of the dissertation, SNR always refers to the total integrated signal and noise power. Assuming that the anti-aliasing filter removes the out-of-band noise and blockers, the system's input SNR can be defined as,

$$\text{SNR}_{\text{input}} = V_{\text{sig},\text{input}}^2 / V_{N,\text{IN}}^2, \quad (5.1)$$

where  $V_{\text{sig},\text{input}}^2$  is the total input signal power and  $V_{N,\text{IN}}^2$  is the total input source noise power over the signal bandwidth  $BW$ . The output SNR of the system is defined by,

$$\text{SNR}_{\text{output}} = V_{\text{sig},\text{output}}^2 / V_{N,\text{OUT}}^2, \quad (5.2)$$

where  $V_{\text{sig},\text{output}}^2$  is the total signal power sampled at the output and  $V_{N,\text{OUT}}^2$  is the total integrated noise power at the receiver output, with the following components,

$$V_{N,\text{OUT}}^2 = V_{N,\text{Gm}}^2 + V_{N,\text{OTA}}^2 + V_{N,\text{II}}^2. \quad (5.3)$$

Here  $V_{N,II}^2$  is induced by the input source noise  $V_{N,IN}^2$  while  $V_{N,Gm}^2$  and  $V_{N,OTA}^2$  are the output referred additive noise due to the RF-Gm stage and baseband OTA. Defining the noise gain and the signal gain as  $|Gain_N|^2 = V_{N,II}^2 / V_{N,IN}^2$  and  $|Gain_S|^2 = V_{sig,output}^2 / V_{sig,input}^2$ , the Noise Figure of the whole front-end  $NF_A$  is given by,

$$\begin{aligned} NF_A &= 10\log\left(\text{SNR}_{\text{input}} / \text{SNR}_{\text{output}}\right) \\ &= 10\log\left(1 + \beta + \mu + \eta\right), \end{aligned} \quad (5.4)$$

Where

$$\mu = V_{N,OTA}^2 / \left(|Gain_S|^2 V_{N,IN}^2\right) \quad (5.5)$$

$$\eta = V_{N,Gm}^2 / \left(|Gain_S|^2 V_{N,IN}^2\right) \quad (5.6)$$

$$\beta = \left(|Gain_N|^2 - |Gain_S|^2\right) / |Gain_S|^2. \quad (5.7)$$

$\mu$  and  $\eta$  represents the SNR degradation due to the OTA and the Gm stage, respectively.  $\beta$  is determined by the difference between the noise gain and the signal gain. The front-end gain is sensitive to the spectrum distribution of the signal according to (3.4). Since often the noise and the signal have different spectrum distributions, then the noise gain is usually not equal to the signal gain.

The parameters in equation (5.5)-(5.7) are quantified as follows. We mainly consider the impact of both thermal and flicker noise sources.

a) Noise from the Gm stage

The simplified noise analysis of the Gm stages is presented in this section. A more detailed mathematical analysis is provide in section 5.4.

The blocking capacitor in Fig.3.6 removes the majority of the flicker noise generated in the Gm stages so only thermal noise is considered. Noise current outputting the Gm stage is mixed with the PN sequence and then integrated in  $C_s$ . By integrating the convolution of the Gm noise and the PN sequence shaped by the Sinc integrator in frequency domain, the total Gm-induced thermal noise power at the receiver output is given by,

$$V_{N,Gm}^2 = \frac{1}{2} K_f \zeta(\rho) \left( \frac{1}{C_s} \right)^2 T_i k T Gm n_{f,Gm}, \quad (5.8)$$

where  $K_f$  is the technology-dependant noise factor and  $n_{f,Gm}$  is the additive noise factor depending on the circuit topology. For the employed 90nm CMOS process,  $K_f$  is 2.7. If an NMOS transistor is used as the main amplifying transistor biased by a PMOS,  $n_{f,Gm}$  is around 1.3.  $T_i$  is the duration of the sampling phase and  $\zeta(\rho)$  is a numerical function depending on the normalized noise bandwidth  $\rho$ ,

$$\rho = \omega_N / 2\pi f_{clk}, \quad (5.9)$$

where  $\omega_N$  is the bandwidth of the noise current due to the Gm stage, according to (3.11) we have,

$$\omega_N = (gm_2 - gm_1) / 2\pi C_p. \quad (5.10)$$

$\zeta(\rho)$  is plotted in Fig.5.1. For example, when  $\omega_N$  is equal to  $2\pi f_{clk}$ ,  $\zeta(\rho) = \zeta(1) \approx 0.82$ , then we have,

$$V_{N,Gm}^2 \approx 0.41 K_f \left( \frac{1}{C_s} \right)^2 T_i k T G_m n_{f,Gm}. \quad (5.11)$$

Substituting equations (3.8) and (5.8) into (5.6), with  $f_{clk}$  being twice the signal bandwidth, yields,

$$\eta = K_f n_{f,Gm} k T \frac{\zeta(\rho)}{\lambda \cdot G_m V_{N,IN}^2}, \quad (5.12)$$

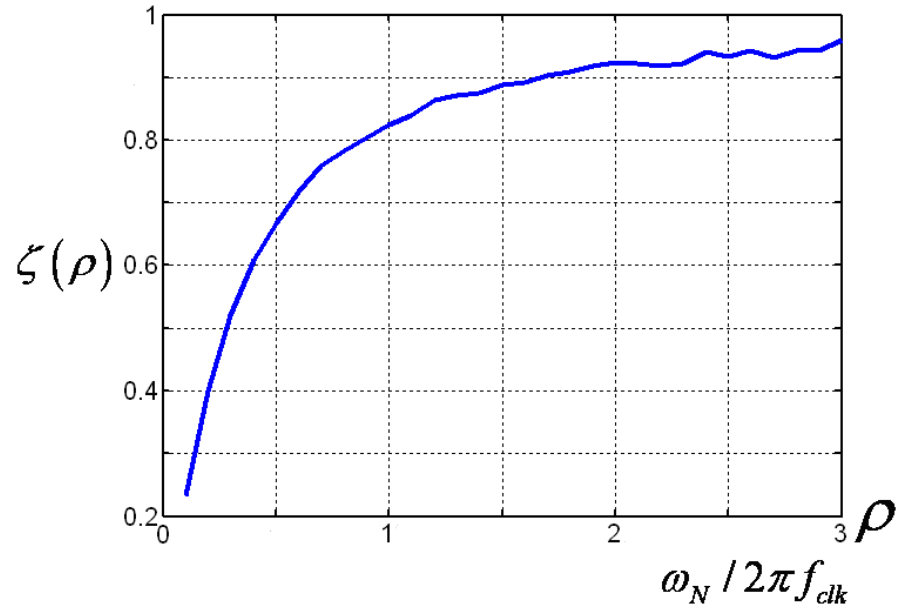


Fig. 5.1  $\zeta(\rho)$  vs.  $\omega_N$

where  $\overline{V_{N,IN}^2}$  is the input source thermal noise density. The impact of the Gm stages in terms of Noise Figure is similar to that in the conventional receiver, but scaled by  $\zeta$  and  $\lambda$ . The equation (5.8) is derived in section 5.4 in details.

#### b) Noise from the OTA

The simplified noise analysis of the OTAs is presented in this section. A more detailed mathematical analysis is provide in section 5.5.

Part of the high frequency thermal noise folds over the baseband spectrum due to the sampling operation and cannot be filtered by the subsequent filters. This sets the fundamental noise floor in  $C_S$  and limits the maximum achievable SNR of the whole system [26]. In this section, the noise floor introduced by thermal and flicker noise sources are quantified.

Referring to Fig. 3.1, when the sampling switch S is ON, the single-ended equivalent circuit around the OTA is shown in Fig. 5.2.  $R_{O,Gm}$  in the figure represents the series of the output resistor of the Gm stage and switch resistance. At the end of the integration, when the sampling switch is turned OFF, the stored noise in  $C_S$  is equal to the total integrated noise in  $C_S$  over the entire bandwidth. Assuming  $R_{O1}$  is comparable with  $R_{O2}$  and  $gm_1 R_{O1} \gg 1$ ,  $gm_2 R_{O2} \gg 1$ , the stored thermal noise in  $C_S$  is given by,

$$V_{Therm.N,C_S}^2 \approx \frac{1}{4} K_f n_{f1} kT \frac{1}{C_S} \frac{R_{O1}}{R_{O,Gm}} gm_2 R_{O2}, \quad (5.13)$$



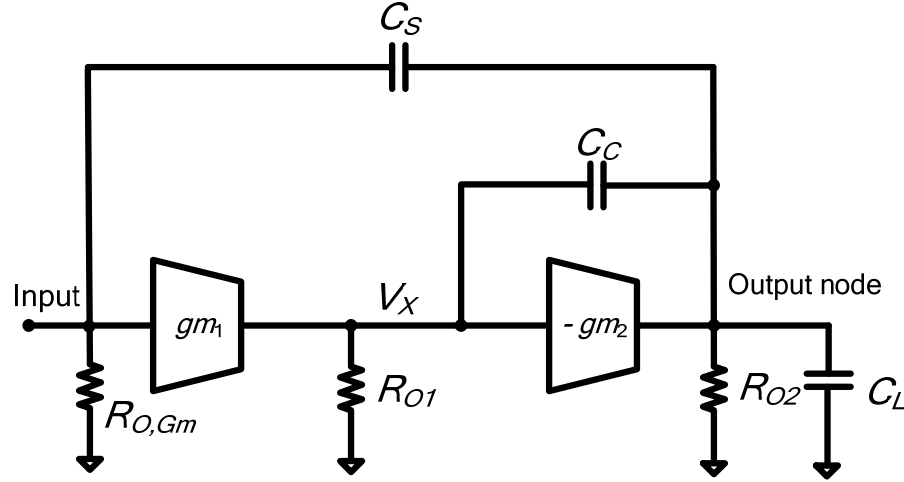


Fig. 5.2 Active integrator equivalent circuit when sampling switch S is ON

where  $n_{f1}$  is the additive noise factor of the first OTA stage, which is around 1.3 for this design. Since  $V_{ThermN,Cs}^2$  is stored in  $C_S$ , it adds to the noise generated when S is OFF.

When the sampling switch S is OFF and the ‘read’ switch is ON, the  $R_{O,Gm}$  is removed and  $C_L$  is dominated by the sampling capacitor of the following ADC denoted as  $C_{L,ADC}$ .

Assuming  $gm_1 R_{O1} \gg 1$ , and  $\frac{C_C}{C_{L,ADC}} \frac{gm_1}{gm_2} \ll 1$ , the total integrated thermal noise at the

output node is computed as,

$$V_{Therm.N,O}^2 = \frac{1}{4} K_f n_{f1} kT \frac{1}{C_C} + \frac{1}{4} K_f n_{f2} kT \frac{1}{C_{L,ADC}}, \quad (5.14)$$

where  $n_{f2}$  is the additive noise factor of the second OTA stage. The first term in (5.14) is due to the first stage, mainly depending on the size of  $C_C$ . The second term is contributed by the second stage and is determined by the size of the input capacitance of the ADC.

Since the OTA's second stage employs a PMOS as the main amplifying transistor  $n_{f2}$  is around 4.3.

According to equations (5.13) and (5.14), the OTA-induced thermal noise that goes to the ADC is given by,

$$V_{Therm.N,OTA}^2 = V_{Therm.N,Cs}^2 + V_{Therm.N,O}^2 \quad (5.15)$$

The flicker noise of the OTA also makes a significant contribution at baseband. Illustrations of the flicker noise, thermal noise and the desired signal at the output of the integrator are shown in Fig. 5.3 (a). The density of the flicker noise can be modeled by a roll-off function  $A/f$ , however it is difficult to predict the amount of flicker noise by a general equation because  $A/f$  is an approximation and the parameter  $A$  depends on both the employed CMOS process technology and circuit parameters such as the transistor gate dimensions and the DC current that feeds the circuit. Flicker noise power in advanced submicron CMOS technology is significant. Simulations show that the total integrated flicker noise is over 10 times stronger than the thermal noise at the output of the integrators. Fortunately, the main part of the flicker noise concentrates at low frequency and can be filtered by a High-Pass Filter (HPF) in the digital domain. Assuming we include a digital HPF after the ADC that removes information in bandwidth 0-5 MHz as shown in Fig.5.3 (b), the flicker noise contribution approximately equals the total integrated thermal noise at the output of the integrator. In order to sample sufficient randomized signal information for the reconstruction, the bandwidth of the integrator needs to increase by 5 MHz in order to keep the same signal bandwidth. Therefore, the low IF signal bandwidth to be sampled is shifted by 5 MHz, so that the

rate of each path ADC needs to increase by 10 MHz. In the proposed receiver, the sampling rate of each ADC is 110 MHz instead of 100 MHz that was predicted in Fig.2.4. System level simulations have confirmed that the sampling scheme in Fig.5.3 (b) has no negative impact on the signal reconstruction compared to that in Fig. 5.3(a).

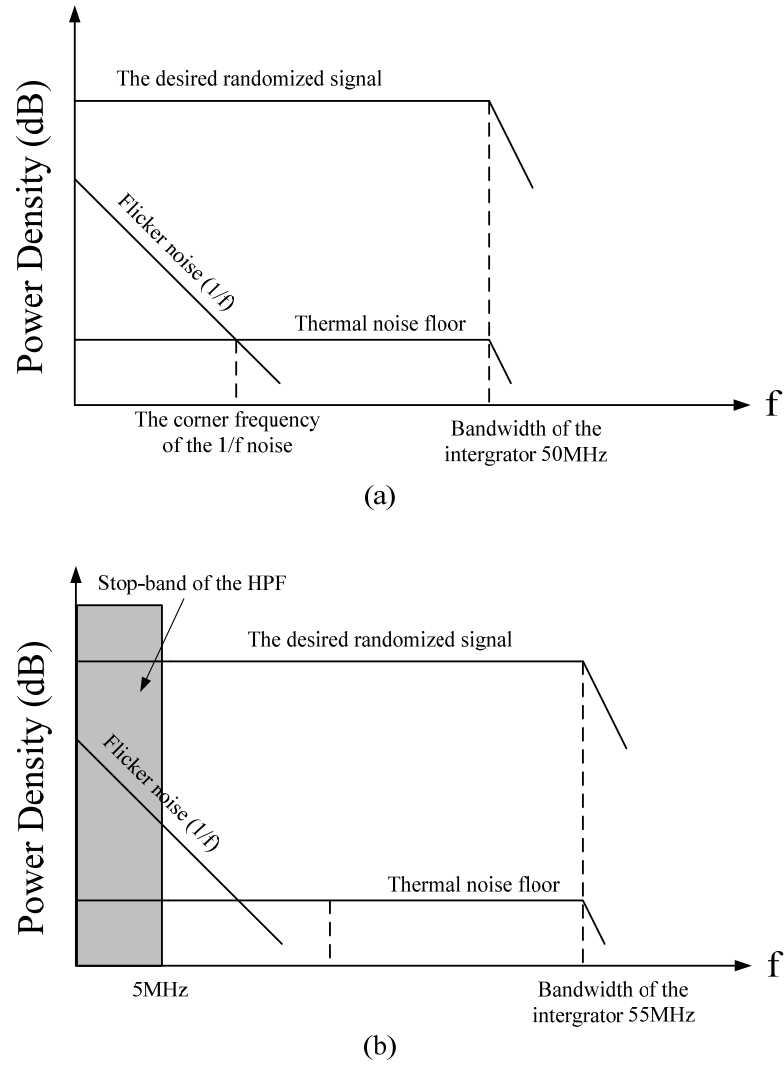


Fig. 5.3 (a) Illustrations of the flicker noise, thermal noise and the desired signal

(b) The signal baseband is shifted by 5MHz

Considering both thermal noise and flicker noise,  $V_{N,OTA}^2$  in equation (5.5) is given by,

$$V_{N,OTA}^2 = \chi V_{Therm.N,OTA}^2, \quad (5.16)$$

where  $V_{Therm.N,OTA}^2$  is the thermal noise given by (5.15) and  $\chi$  is an additive factor due to the flicker noise that can be reduced by increasing the offset frequency in Fig.5.3 (b), leading to a low IF architecture. In this prototype,  $\chi$  is 1.8 when the frequency offset is 5 MHz. Equations (5.13) and (5.14) are derived in details in section 5.5

c) Noise gain of the front-end  $|Gain_N|^2$

By calculating  $V_{N,II}^2$  in the same way as  $V_{N,Gm}^2$  is calculated, the noise power gain

$|Gain_N|^2$  is given by,

$$\begin{aligned} |Gain_N|^2 &= V_{N,II}^2 / V_{N,IN}^2 \\ &= \zeta(\rho) \left( \frac{1}{C_s} \right)^2 T_i |Gm|^2 \frac{1}{f_{clk}}. \end{aligned} \quad (5.17)$$

$\zeta(\rho)$  depends on the bandwidth of  $V_{N,IN}^2$ . Given that the anti-aliasing filter before the Gm stages removes the out-of-band noise, the bandwidth of  $V_{N,IN}^2$  is equal to the desired signal bandwidth  $BW$ . Typically  $BW$  is half  $f_{clk}$ . Then  $\zeta(\rho) = \zeta(0.5) = 0.67$  and the noise gain is given by,

$$|Gain_N|^2 = 0.67 \left( \frac{1}{C_s} \right)^2 T_i |Gm|^2 \frac{1}{f_{clk}}. \quad (5.18)$$

Substituting (3.8) and (5.18) into (5.7), yields,

$$\beta = \frac{0.67 - \lambda}{\lambda}. \quad (5.19)$$

When the signal is normally distributed, the noise gain equals the signal gain and  $\beta = 0$ .

When most of the signal power is located at low frequency the signal gain is larger than the noise gain and  $\beta < 0$ , while  $\beta > 0$  if the input signal is concentrated at high frequencies, leading to lower SNR figures.

## 5.2 Distortion

The Gm stage introduces non-linearity before the randomization. The most significant issue is the third-order inter-modulation distortion ( $IM_3$ ).  $IIP_3$  (in dB) of the Gm stage represents how much  $IM_3$  is generated. With the input signal power denoted  $P_{in}$  (in dB), the signal to distortion ratio SDR at the output of the Gm stage is equivalent to  $2(IIP_3 - P_{in})$ , and the distortion power is  $3P_{in} - 2IIP_3$  [27]. Assuming the full scale input is  $P_{max}$ , the worst case distortion is  $3P_{max} - 2IIP_3$ . To achieve the desired SDR,  $IIP_3$  needs to be better than  $(3P_{max} - \text{SDR})/2$ .

After the signal randomization at the mixer, the OTA in the active integrator also introduces non-linearity. However, the OTA does not directly distort the input signal. Rather, the OTA distorts elements in the Matrix  $S$  in Fig.2.3, which is the sampled data in  $C_S$ . This alleviates the impact of the OTA-induced distortions, because signal reconstruction in the digital domain applies a random matrix, which is the inverse of the

applied PN sequences, to the sampled data  $S$ . This randomizes the OTA-induced distortion in  $S$ . In the reconstructed signal spectrum, the randomized distortions appear as broad band random noise, and there are no significant spurious tones. Thus the ultimate impact of distortion from the OTA is similar to that caused by analog thermal noise. The amount of introduced noise power is equal to the power of the distortion generated by the active integrator. SDR at the integrator needs to be better than the targeted SNDR, so that the reconstructed noise floor does not rise.

### 5.3 Other non-idealities

Although the digital PN sequences are known, their analog waveforms are distorted by several unavoidable non-idealities such as clock timing offset and charge leakage at the sampler. Thus, a calibration step is necessary to obtain the actual matrix  $\mathbf{V} = \Phi \psi^H$  needed for signal reconstruction. To accomplish this, priori known single tone signals may be transmitted through the system to measure the system output response. Thus, the matrix  $\Phi \psi^H$  obtained will include the effect of all the linear time-invariant errors in the front-end [28]. The calibration scheme is explained in details in chapter VI. It is preferred to design a fully differential front-end to make it more tolerant to clock feed-through, power supply noise and other common-mode noise sources.

#### 5.4 The mathematical derivations of the noise from the Gm stages

The Gm stage generates thermal noise current  $\overline{I_{N,Gm}^2(f)}$  at its output, given by

$$\overline{I_{N,Gm}^2(f)} = K_f kTGm \cdot n_{f,Gm} \frac{1}{\left|1 + j2\pi f / \omega_N\right|^2} \quad (5.20)$$

where  $\omega_N$  is the -3 dB noise bandwidth. According to equation (3.11),  $\omega_N = \frac{gm_2 - gm_1}{2\pi C_p}$ .

$K_f$  is a parameter depending on the process. It is equal to 2.7 with IBM 90nm CMOS process. Before going into the integrator this noise is mixed with the PN sequence. Let the power density of the PN sequence be  $\overline{PN^2(f)}$ , given by

$$\overline{PN^2(f)} \approx \frac{1.8}{f_{clk}} \left| \text{Sinc}\left(\frac{\pi f}{f_{clk}}\right) \right|^2, \quad (5.21)$$

where  $f_{clk}$  is the clock frequency of the PN generator.

Now, let the noise current density after the mixer be  $\overline{I_{N,mixed}^2(f)}$ , so

$$\overline{I_{N,mixed}^2(f)} = \int_{-\infty}^{\infty} \overline{I_{N,Gm}^2(f - \eta)} \overline{PN^2(\eta)} d\eta. \quad (5.22)$$

$\overline{I_{N,mixed}^2}$  enters the integrator and is shaped by the sinc type low pass filter  $H_{int}(f)$ .

Assume the noise density at the output is  $\overline{V_{N,out}^2(f)}$ , then

$$\overline{V_{N,out}^2(f)} = \overline{I_{N,mixed}^2(f)} \left| H_{int}(f) \right|^2$$

$$= \overline{I_{N,mixed}^2(f)} \left| \frac{T_i}{C_s} \text{Sinc}(\pi f \cdot T_i) \right|^2. \quad (5.23)$$

At the end of the integration window, the sampling switch S turns off and the noise power is sampled and conserved in  $C_s$ , so that the noise power over the entire bandwidth folds back into the signal band. Let the overall integrated noise power at the output be

$$V_{N,out}^2,$$

$$V_{N,out}^2 = \int_0^\infty \overline{I_{N,mixed}^2(f)} \left| \frac{T_i}{C_s} \text{Sinc}(\pi f T_i) \right|^2 df. \quad (5.24)$$

Because the -3 dB bandwidth of the sinc filter  $1/2T_i$  is usually much smaller than the bandwidth of  $\overline{I_{N,mixed}^2(f)}$ , the noise is almost constant in the band of interest. We

assume  $\overline{I_{N,mixed}^2(f)}|_{f \rightarrow 0} \approx N\_D$ , where  $N\_D$  is the density of  $\overline{I_{N,mixed}^2(f)}$  at very low frequency. Now,

$$V_{N,out}^2 = \int_0^\infty N\_D \left| \frac{T_i}{C_s} \text{Sinc}(\pi f T_i) \right|^2 df \approx \left( \frac{1}{C_s} \right)^2 \frac{T_i}{2} N\_D. \quad (5.25)$$

A closed form expression for  $N\_D$  is not available due to the convolution in  $\overline{I_{N,mixed}^2(f)}$ , so system level simulation is employed to explore the relationship between  $N\_D$  and critical design parameters.  $N\_D$  versus  $\omega_N / 2\pi f_{CLK}$  is simulated and  $N\_D$  is given by,

$$N\_D = \zeta \cdot K_f kTGm \cdot n_{f,Gm} \quad (5.26)$$

$\zeta$  is plotted in Fig.5.1. The output noise power is given by,



$$V_{N,Gm}^2 = \frac{1}{2} K_f \zeta \left( \frac{1}{C_s} \right)^2 T_i k T G m n_{f,Gm} \quad (5.8)$$

### 5.5 The mathematical derivations of the noise from the OTAs.

A useful equation is given here before the derivations,

$$\int_0^\infty \left| \frac{n_2 s^2 + n_1 s + n_0}{d_3 s^3 + d_2 s^2 + d_1 s + d_0} \right|_{s=j\omega}^2 df = \frac{1}{4} \frac{n_2^2 d_1 d_0 + n_1^2 d_3 d_0 + n_0^2 d_3 d_2 - 2 n_2 n_0 d_3 d_0}{d_3 (d_2 d_1 - d_3 d_0) d_0} \quad (5.27)$$

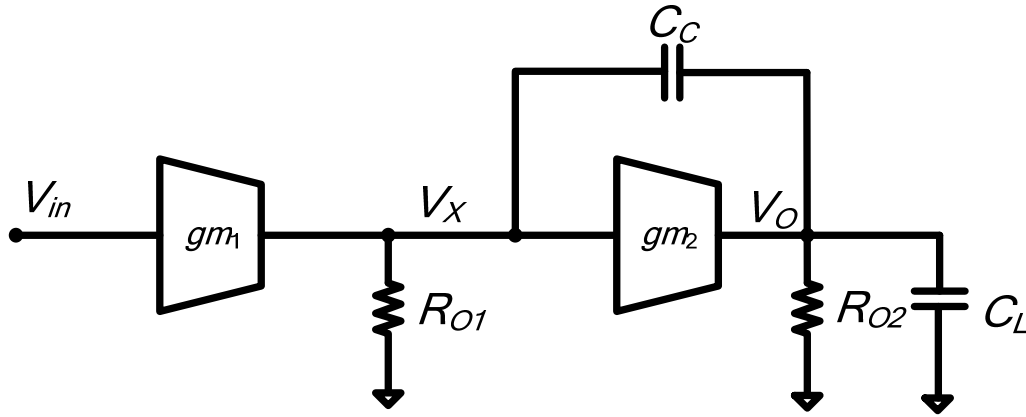


Fig. 5.4 The small signal model of the two stage OTA

The open loop gain of the two stage OTA shown in Fig. 5.4 is derived as bellows.

$$V_{in} g m_1 = -\frac{V_X}{R_{O1}} - s C_C (V_X - V_O) \quad (5.28)$$

$$V_X g m_2 = s C_C (V_X - V_O) - \frac{V_O}{R_{O2}} - s C_L V_O \quad (5.29)$$

$$(5.28) \Rightarrow V_x = \frac{sC_C R_{O1} V_o - V_{in} g_{m1} R_{O1}}{1 + sC_C R_{O1}} \quad (5.30)$$

Substitute (5.30) into (5.29),

$$\begin{aligned} \frac{sC_C R_{O1} V_o - V_{in} g_{m1} R_{O1}}{1 + sC_C R_{O1}} g_{m2} &= sC_C \left( \frac{sC_C R_{O1} V_o - V_{in} g_{m1} R_{O1}}{1 + sC_C R_{O1}} - V_o \right) - \frac{V_o}{R_{O2}} - sC_L V_o \\ \Rightarrow \frac{V_o}{V_{in}} &= \frac{g_{m1} R_{O1} g_{m2} R_{O2} \left( 1 - \frac{sC_C}{g_{m2}} \right)}{s^2 C_C R_{O1} C_L R_{O2} + s(C_C R_{O1} g_{m2} R_{O2} + C_L R_{O2} + C_C R_{O2} + C_C R_{O1}) + 1} \\ &\approx \frac{g_{m1} R_{O1} g_{m2} R_{O2} \left( 1 - \frac{sC_C}{g_{m2}} \right)}{s^2 C_C R_{O1} C_L R_{O2} + s(C_C R_{O1} g_{m2} R_{O2} + C_L R_{O2}) + 1} \end{aligned} \quad (5.31)$$

The overall transconductance of the two stage OTA is derived as bellows. Assume the output node is grounded, then,

$$V_{in} g_{m1} = -\frac{V_x}{R_{O1}} - sC_C V_x \Rightarrow -V_{in} \frac{g_{m1} R_{O1}}{1 + sC_C R_{O1}} = V_x \quad (5.32)$$

$$I_{out} = V_x g_{m2} - sC_C V_x \Rightarrow I_{out} = -V_{in} \frac{g_{m2} g_{m1} R_{O1}}{1 + sC_C R_{O1}} + V_{in} \frac{sC_C g_{m1} R_{O1}}{1 + sC_C R_{O1}} \quad (5.33)$$

$$\Rightarrow g_{m_{eq}} = g_{m2} \frac{g_{m1} R_{O1} \left( s \frac{C_C}{g_{m2}} - 1 \right)}{1 + sC_C R_{O1}} \quad (5.34)$$

Referring to Fig.3.1, when the sampling switch is turned off, the equivalent circuit is shown in Fig.5.5. The parasitic capacitor at the input of the OTA is ignored.

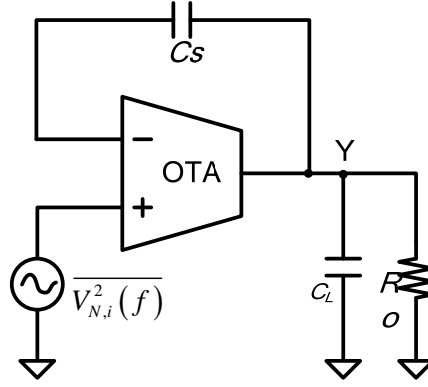


Fig. 5.5 Active integrator equivalent circuit when sampling switch is off

Let  $\overline{V_{N1,i}^2(f)}$  be the input referred noise voltage density of the first stage and  $\overline{V_{N2,i}^2(f)}$  be the input referred noise voltage density of the second stage, the overall input referred noise is  $\overline{V_{N,i}^2(f)}$ ,

$$\overline{V_{N1,i}^2(f)} = K_f n_{f1} \frac{kT}{gm_1} \quad (5.35)$$

$$\overline{V_{N2,i}^2(f)} = \frac{K_f n_{f2} kT gm_2}{gm_{eq}^2} \quad (5.36)$$

Substitute (5.34) into (5.36), we have,

$$\overline{V_{N2,i}^2(f)} = \frac{K_f n_{f2} kT}{gm_2 \left( \frac{gm_1 R_{O1} \left( s \frac{C_c}{gm_2} - 1 \right)}{1 + s C_c R_{O1}} \right)^2} \quad (5.37)$$

Then we have,

$$\overline{V_{N,i}^2(f)} = K_f n_{f1} \frac{kT}{gm_1} + \frac{K_f n_{f2} kT}{gm_2 \left( \frac{gm_1 R_{O1} \left( s \frac{C_c}{gm_2} - 1 \right)}{1 + s C_c R_{O1}} \right)^2} \quad (5.38)$$

Where  $n_{f1}$  is the additive noise factor of the first OTA stage and  $n_{f2}$  the noise factor of the second stage. Let  $H_n(f)$  be the closed loop noise transfer function from  $\overline{V_{N,i}^2(f)}$  to the output node Y, given by

$$\begin{aligned} H_n(f) &= \frac{\frac{gm_1 R_{O1} gm_2 R_{O2} \left( 1 - \frac{s C_c}{gm_2} \right)}{s^2 C_c R_{O1} C_L R_{O2} + s (C_c R_{O1} gm_2 R_{O2} + C_L R_{O2}) + 1}}{1 + \frac{gm_1 R_{O1} gm_2 R_{O2} \left( 1 - \frac{s C_c}{gm_2} \right)}{s^2 C_c R_{O1} C_L R_{O2} + s (C_c R_{O1} gm_2 R_{O2} + C_L R_{O2}) + 1}} \\ H_n(f) &= \frac{gm_1 R_{O1} gm_2 R_{O2} \left( 1 - \frac{s C_c}{gm_2} \right)}{s^2 C_c R_{O1} C_L R_{O2} + s \left( C_c R_{O1} gm_2 R_{O2} + C_L R_{O2} - \frac{C_c}{gm_2} \right) + gm_1 R_{O1} gm_2 R_{O2} + 1} \\ H_n(f) &\approx \frac{gm_1 R_{O1} gm_2 R_{O2} \left( 1 - \frac{s C_c}{gm_2} \right)}{s^2 C_c R_{O1} C_L R_{O2} + s (C_c R_{O1} gm_2 R_{O2} + C_L R_{O2}) + gm_1 R_{O1} gm_2 R_{O2}} \end{aligned} \quad (5.39)$$

Now  $V_{O,N1}^2$  is the total integrated noise due to the first stage at the output, according to

(5.27),

$$\begin{aligned} V_{O,N1}^2 &= \int_0^\infty H_n(f) \overline{V_{N1,i}^2} df \\ &= K_f n_{f1} \frac{kT}{gm_1} \int_0^\infty \left| \frac{gm_1 R_{O1} gm_2 R_{O2} \left( 1 - \frac{s C_c}{gm_2} \right)}{s^2 C_c R_{O1} C_L R_{O2} + s (C_c R_{O1} gm_2 R_{O2} + C_L R_{O2}) + gm_1 R_{O1} gm_2 R_{O2}} \right|^2 df \end{aligned}$$

$$\begin{aligned}
&= K_f n_{f1} \frac{kT}{gm_1} \int_0^\infty \left| \frac{1 - \frac{sC_c}{gm_2}}{s^2 \frac{C_c C_L}{gm_1 gm_2} + s \frac{C_c R_{o1} gm_2 R_{o2} + C_L R_{o2}}{gm_1 R_{o1} gm_2 R_{o2}} + 1} \right|^2 df \\
&= \frac{1}{4} K_f n_{f1} kT \frac{\frac{C_c}{gm_1} + 1}{\frac{C_L}{gm_2}} \frac{1}{C_c + \frac{C_L}{R_{o1} gm_2}} \quad (5.40)
\end{aligned}$$

Now  $V_{o,N2}^2$  is the total integrated noise due to the second stage at the output, according to

(5.27),

$$\begin{aligned}
V_{o,N2}^2 &= \int_0^\infty H_n(f) \overline{V_{N2,i}^2} df \\
&= \frac{K_f n_{f2} kT}{gm_2 gm_1^2 R_{o1}^2} \int_0^\infty \left| \frac{gm_1 R_{o1} gm_2 R_{o2} (1 + sC_c R_{o1})}{s^2 C_c R_{o1} C_L R_{o2} + s(C_c R_{o1} gm_2 R_{o2} + C_L R_{o2}) + gm_1 R_{o1} gm_2 R_{o2}} \right|^2 df \\
&= \frac{K_f n_{f2} kT}{gm_2 gm_1^2 R_{o1}^2} \int_0^\infty \left| \frac{1 + sC_c R_{o1}}{s^2 \frac{C_c C_L}{gm_1 gm_2} + s \frac{C_c R_{o1} gm_2 + C_L}{gm_1 R_{o1} gm_2} + 1} \right|^2 df \\
&= \frac{1}{4} K_f n_{f2} kT \frac{1}{C_L} \frac{C_c R_{o1} + \frac{C_L}{gm_1 gm_2 R_{o1}}}{C_c R_{o1} + \frac{C_L}{gm_2}} \quad (5.41)
\end{aligned}$$

Equation (5.14) is obtained by summing (5.41) and (5.40) with assumptions such as

$$gm_1 R_{o1} \gg 1, \text{ and } \frac{C_c}{C_{L,ADC}} \frac{gm_1}{gm_2} \ll 1.$$

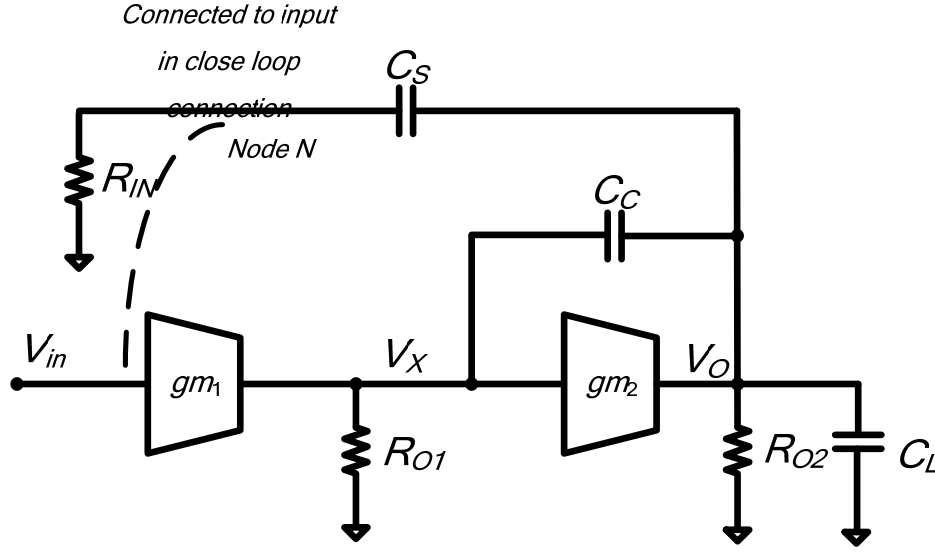


Fig. 5.6 The small signal model of the active integrator when the sampling switch is ON

In Fig.3.1, when the sampling switch is turned ON, the output resistance of the previous stage is presented at the input of the active integrator (Fig.5.6). Here we use  $R_{IN}$  to generally represent this resistance. Assume  $R_{IN}$  is bigger than  $R_{O2}$ , by ignoring loading effects of the feedback path, going through the similar derivations for equation (5.31), we have,

$$\begin{aligned} \frac{V_O}{V_{in}} &= \frac{gm_1 R_{O1} gm_2 R_{O2} \left(1 - \frac{sC_C}{gm_2}\right)}{s^2 C_C R_{O1} C_L R_{O2} + s(C_C R_{O1} gm_2 R_{O2} + C_L R_{O2} + C_C R_{O2} + C_C R_{O1}) + 1} \\ \Rightarrow \frac{V_O}{V_N} &= \frac{gm_1 R_{O1} gm_2 R_{O2} \left(1 - \frac{sC_C}{gm_2}\right)}{s^2 C_C R_{O1} C_L R_{O2} + s(C_C R_{O1} gm_2 R_{O2} + C_L R_{O2} + C_C R_{O2} + C_C R_{O1}) + 1} \frac{sC_S R_{IN}}{sC_S R_{IN} + 1} \quad (5.42) \end{aligned}$$

Let  $H_n(f)$  be the closed loop noise transfer function from the input to the voltage across  $C_S$ , given by,

$$\begin{aligned}
H_n(f) &= \frac{\frac{gm_1 R_{O1} gm_2 R_{O2} \left(1 - \frac{sC_c}{gm_2}\right)}{s^2 C_c R_{O1} C_L R_{O2} + s(C_c R_{O1} gm_2 R_{O2} + C_L R_{O2} + C_c R_{O2} + C_c R_{O1}) + 1} \frac{1}{sC_s R_{IN} + 1}}{1 + \frac{\frac{gm_1 R_{O1} gm_2 R_{O2} \left(1 - \frac{sC_c}{gm_2}\right)}{s^2 C_c R_{O1} C_L R_{O2} + s(C_c R_{O1} gm_2 R_{O2} + C_L R_{O2} + C_c R_{O2} + C_c R_{O1}) + 1} \frac{sC_s R_{IN}}{sC_s R_{IN} + 1}} \\
\Rightarrow H_n(f) &\approx \frac{gm_1 R_{O1} gm_2 R_{O2} \left(1 - \frac{sC_c}{gm_2}\right)}{s^3 C_s R_{IN} C_c R_{O1} C_L R_{O2} + s^2 C_s R_{IN} C_c R_{O1} R_{O2} (gm_2 - gm_1) + sC_s R_{IN} gm_1 R_{O1} gm_2 R_{O2} + 1} \quad (5.43)
\end{aligned}$$

Now  $V_{Cs,N1}^2$  is the total integrated noise on  $C_s$  due to the first stage, according to (5.27),

$$\begin{aligned}
V_{Cs,N1}^2 &= \int_0^\infty H_n(f) \overline{V_{N1,i}^2} df \\
&= K_f n_{f1} \frac{kT}{gm_1} \int_0^\infty \left| \frac{gm_1 R_{O1} gm_2 R_{O2} \left(1 - \frac{sC_c}{gm_2}\right)}{s^3 C_s R_{IN} C_c R_{O1} C_L R_{O2} + s^2 C_s R_{IN} C_c R_{O1} R_{O2} (gm_2 - gm_1) + sC_s R_{IN} gm_1 R_{O1} gm_2 R_{O2} + 1} \right|^2 df \\
&= K_f n_{f1} kT gm_1 gm_2^2 R_{O2}^2 R_{O1}^2 \int_0^\infty \left| \frac{1 - \frac{sC_c}{gm_2}}{s^3 C_s R_{IN} C_c R_{O1} C_L R_{O2} + s^2 C_s R_{IN} C_c R_{O1} R_{O2} (gm_2 - gm_1) + sC_s R_{IN} gm_1 R_{O1} gm_2 R_{O2} + 1} \right|^2 df \\
&= \frac{1}{4} K_f n_{f1} kT gm_1 gm_2^2 R_{O2}^2 R_{O1}^2 \frac{\frac{C_c^2}{gm_2^2} + C_s R_{IN} C_c R_{O1} R_{O2} (gm_2 - gm_1)}{C_s R_{IN} C_c R_{O1} R_{O2} (gm_2 - gm_1) C_s R_{IN} gm_1 R_{O1} gm_2 R_{O2} - C_s R_{IN} C_c R_{O1} C_L R_{O2}} \\
&\approx \frac{1}{4} K_f n_{f1} kT \frac{1}{C_s} \frac{R_{O1}}{R_{IN}} gm_2 R_{O2} \quad (5.44)
\end{aligned}$$

Now  $V_{Cs,N2}^2$  is the total integrated noise due to the second stage at the output, according to

(5.27),

$$\begin{aligned}
V_{Cs,N2}^2 &= \int_0^\infty H_n(f) \overline{V_{N2,i}^2} df \\
&= K_f n_{f2} kT g m_2 R_{O2}^2 \int_0^\infty \left| \frac{1 + s C_C R_{O1}}{s^3 C_S R_{IN} C_C R_{O1} C_L R_{O2} + s^2 C_S R_{IN} C_C R_{O1} R_{O2} (g m_2 - g m_1) + s C_S R_{IN} g m_1 R_{O1} g m_2 R_{O2} + 1} \right|^2 df \\
&= K_f n_{f2} kT g m_2 R_{O2}^2 \frac{C_C^2 R_{O1}^2 + C_S R_{IN} C_C R_{O1} R_{O2} (g m_2 - g m_1)}{C_S R_{IN} C_C R_{O1} R_{O2} (g m_2 - g m_1) C_S R_{IN} g m_1 R_{O1} g m_2 R_{O2} - C_S R_{IN} C_C R_{O1} C_L R_{O2}} \\
&\approx \frac{1}{4} K_f n_{f2} kT \frac{1}{C_S} \frac{R_{O2}}{R_{IN}} \frac{1}{g m_1 R_{O1}} \tag{5.45}
\end{aligned}$$

Comparing (5.45) with (5.44), the noise given by the first stage is usually dominant. We got equation (5.13) by replacing  $R_{IN}$  with  $R_{O,Gm}$  in (5.44).



## CHAPTER VI

### THE DESIGN PROCEDURE AND SIMULATIONS

#### 6.1 Specifications of critical blocks and block level simulations

A CS front-end circuit was designed in the IBM 90nm CMOS technology. In simulation 0.5 ps state of art jitter variance is assumed and the system targets for 44 dB (7 bits) reconstructed signal quality. Performance of key circuit blocks and the power consumption are estimated by post-layout simulations. Parasitic extractions and simulations were done with Calibre and Cadence Spectre. The outputs of the front-end are connected to buffers that drive the external ADCs' loading capacitance  $C_{LADC}$ . The external ADCs' may be implemented on the PCB or emulated by digital oscilloscopes. In the simulations, a capacitor is inserted at the output of the integrator to emulate the ADCs' loading. The power consumption of the testing-purpose buffers is not included. System level design specs are listed in Table 6.1.

For 50 ohms input impedance matching  $V_{N,IN}^2$  is equivalent to  $-174\text{dBm/Hz} \times BW$ , which corresponds to  $-82.24\text{ dBm}$  when integrated in  $BW=1.5\text{ GHz}$ . In the proposed receiver  $V_{sig,input}^2$  is expected to be  $-20\text{ dBm}$  and  $\text{SNR}_{input}$  is around  $62\text{ dB}$ . The noise figure of the front-end is  $12\text{ dB}$  to achieve  $50\text{ dB SNR}$ .  $|Gain_s|^2$  is around  $20\text{ dB}$  to amplify the input signal up to the range of  $0\text{ dBm}$ .

Assuming  $R_{01}$  is comparable with  $R_{0,Gm}$  and  $gm_2 R_{02} \cong 10$ , according to equations (5.13)-(5.15),  $C_S$ ,  $C_C$ , and  $C_{LADC}$  needs to be  $500\text{ fF}$ ,  $50\text{ fF}$  and  $165\text{ fF}$  to set up an

Table 6.1 Design specs of the CS front-end

Input Signal Bandwidth	10 MHz ~ 1.5 GHz
Number of Parallel Paths	8
Single Path sampling rate (10/256 signal sparsity)	110 Ms/s
Overall System Sampling rate	880 MS/s (29% Nyquist Rate)
SNDR with 0.5 ps jitter	44 dB
Max. signal gain at the front-end	around 20 dB
Fullscale input / output	-20 dBm / -2 dBm (referred to 50 ohms)  0.06 / 0.5V <sub>pp</sub>

overall thermal noise floor such that  $SNR > 50$  dB. Leaving 3 dB design margin for the flicker noise, we used  $C_S$  of 1 pF and  $C_{L,ADC}$  of 330 fF while  $C_C$  is 300 fF to get enough OTA phase margin for the OTAs. The transfer function (Magnitude and phase) of the designed OTA is shown in Fig.6.1. The OTA used in the active integrator achieves 37 dB DC gain and  $GBW$  of 251 MHz with 1.2 mW power consumption while driving  $C_S$  and  $C_{L,ADC}$ . The phase margin is 69 degrees. The worst case SDR of the active integrator is around 52.8 dB when a full scale signal is applied. According to simulations the OTA

induced noise is -52 dB with reference to the full scale signal when flicker noise between 0~5 MHz is not accounted. The contribution of flicker noise above 5 MHz is 44 %. The noise contributions are distributed as shown in Fig.6.2.

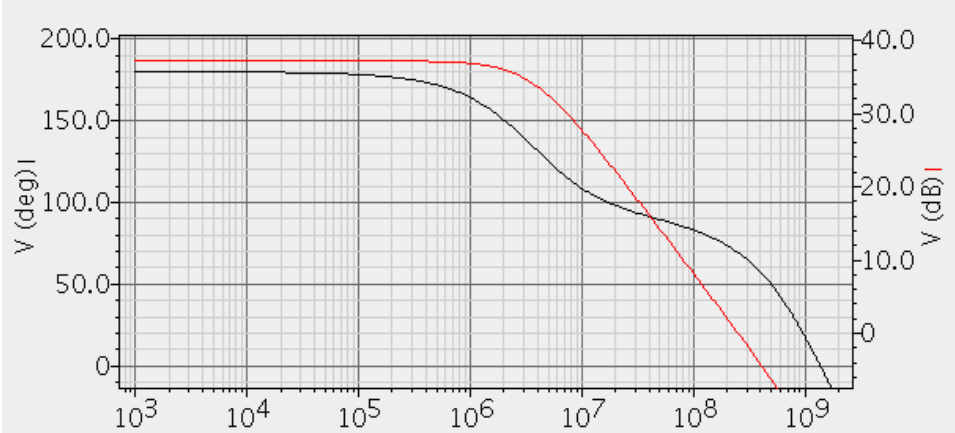


Fig.6.1 The Bode plot of the OTA

Device	Param	Noise Contribution	% Of Total
/I0/MT6	id	6.1094e-09	3.07
/I0/MT504	id	6.10827e-09	3.07
/I0/MT602	id	6.08011e-09	3.06
/I0/MT503	id	6.07794e-09	3.06
/I0/MT603	id	6.04717e-09	3.04
/I0/MT502	id	6.04439e-09	3.04
/I0/MT604	id	5.98188e-09	3.01
/I0/MT5	id	5.97908e-09	3.01
/I0/MT504	fn	5.23819e-09	2.63
/I0/MT6	fn	5.23626e-09	2.63
/I0/MT4	id	5.22833e-09	2.63
/I0/MT102	id	5.22814e-09	2.63
/I0/MT1	id	5.2115e-09	2.62
/I0/MT402	id	5.21096e-09	2.62
/I0/MT602	fn	5.20359e-09	2.62
/I0/MT503	fn	5.20352e-09	2.62
/I0/MT603	fn	5.14386e-09	2.59
/I0/MT502	fn	5.14328e-09	2.59
/I0/MT604	fn	5.02269e-09	2.53
/I0/MT5	fn	5.02206e-09	2.53
Integrated Noise Summary (in V^2) Sorted By Noise Contributors			
Total Summarized Noise = 1.9889e-07			
No input referred noise available			
The above noise summary info is for noise data			

Fig.6.2 The noise contribution distributions in the active integrator

The Gm stages achieve  $G_m=6.5$  mS and  $IIP_3=6$  dBm (referred to 50 ohm) with a power consumption of 2 mW. The Gm stages used in the 8 parallel paths consume 16 mW. The SDR is 52 dB for an input signal power of -20 dBm. The simulated  $NF$  of each Gm stage is 10.2 dB. In the CS receiver, the Gm induced noise factor needs to be scaled by  $\zeta/\lambda$ , finally resulting in  $NF$  of 11.1 dB assuming  $\zeta$  is 0.82 and  $\lambda$  is 0.67. A plot of the  $NF$  over frequencies is shown in Fig.6.3.

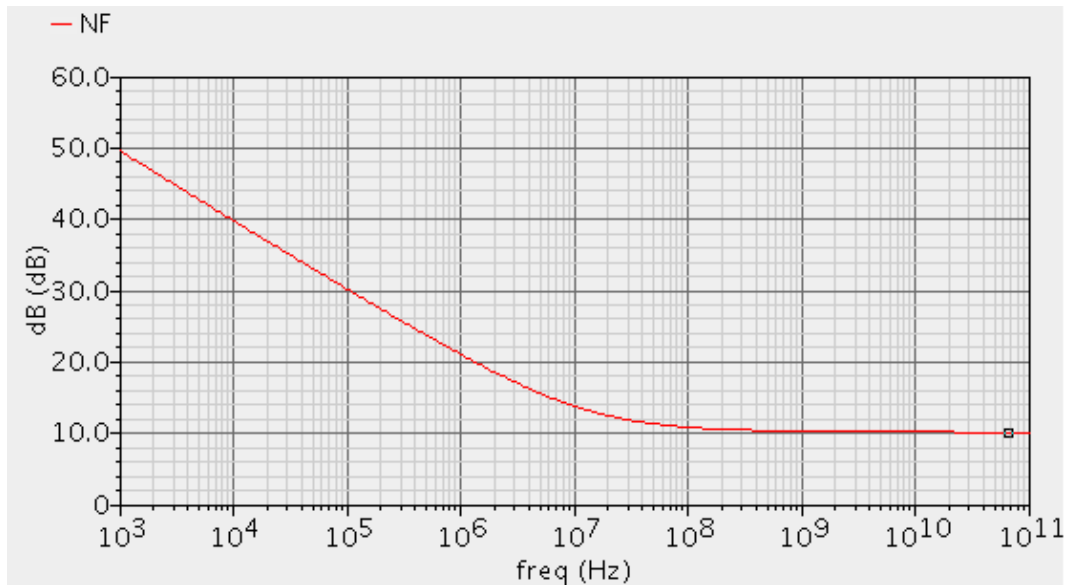


Fig.6.3 Noise Figure of the designed Gm stage

A single PN generator that operates up to 3 GHz is designed with the employed 90nm CMOS technology. A screen shot of the PN sequence obtained through Cadence is shown in Fig. 6.4. The screen shot of the PN spectrum in simulation is shown in Fig.6.5. All the digital clocking circuits consume 57.6 mW.

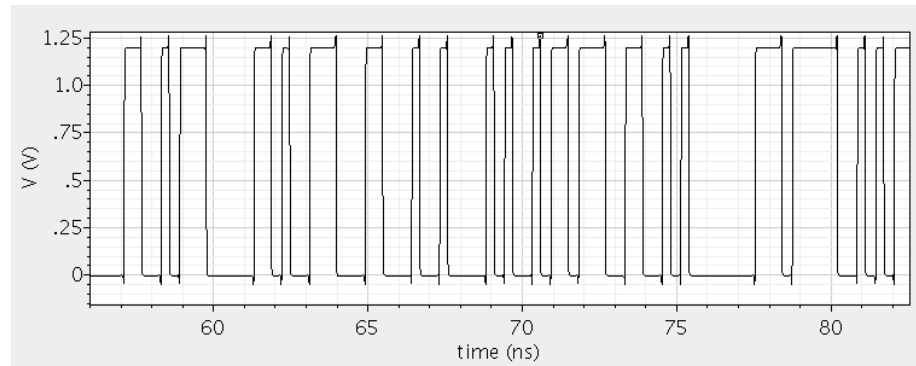


Fig. 6.4 Example of the PN sequence

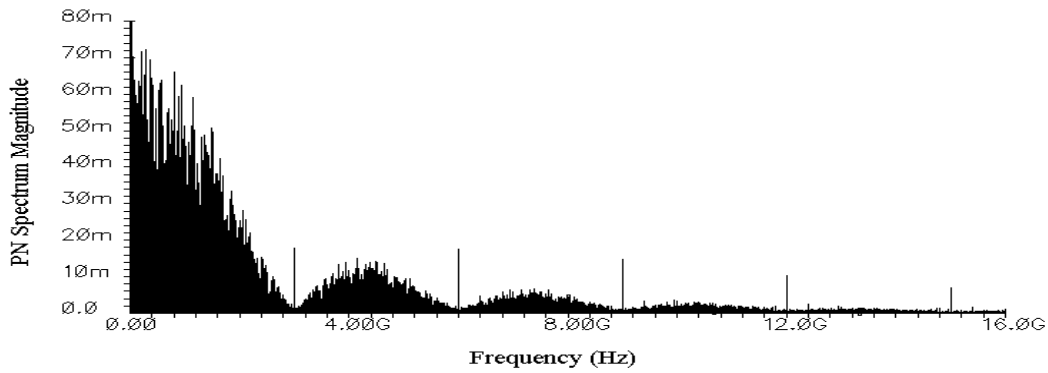


Fig. 6.5 The spectrum of the PN sequence at 3GHz data rate

At the final output of a single path, the output waveform looks like a few steps (Fig.6.6), each of which at the ‘read’ phase is a sampled data that forms the Matrix  $S$ . The output nodes are actually floating at the ‘reset’ phase. At that time the voltage is determined by the previous output and the charge injection from switches. The data at the moment is not usable. Useful data at ‘read’ phases are sampled by the following ADCs.

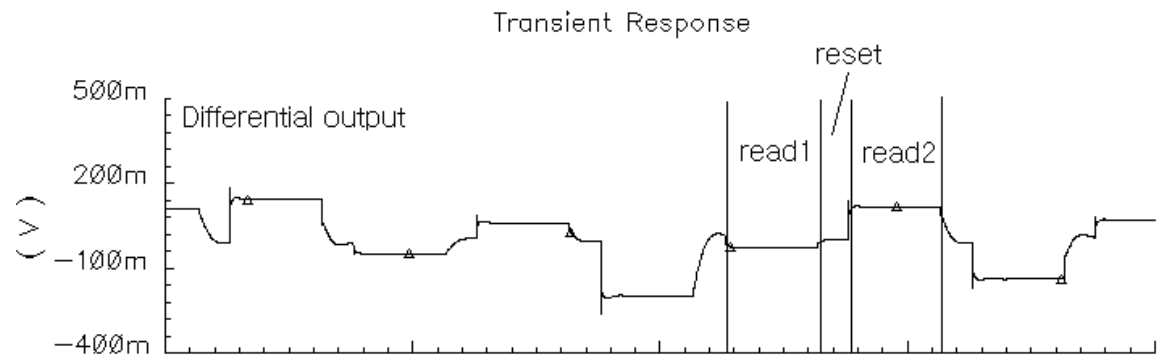


Fig. 6.6 The waveform of the output of a single path

Power consumption of the proposed system is summarized in Table 6.2, with power of ADCs included, as estimated in Section 3-2. According the block level simulations shown above, 7 bits SNR is achievable with this front-end. The layout of a single path is shown in Fig.6.7. The overall chip area for 8 paths is estimated to be 1000um x 1400um.

Table 6.2 Compressive sensing system power summary

Power consumption @ 800 Ms/s	Gm stages	16 mW
	Integrators	19.2 mW
	Clocks	57.6 mW
	PN sequences	
	ADCs	28 mW
	Overall	120.8 mW

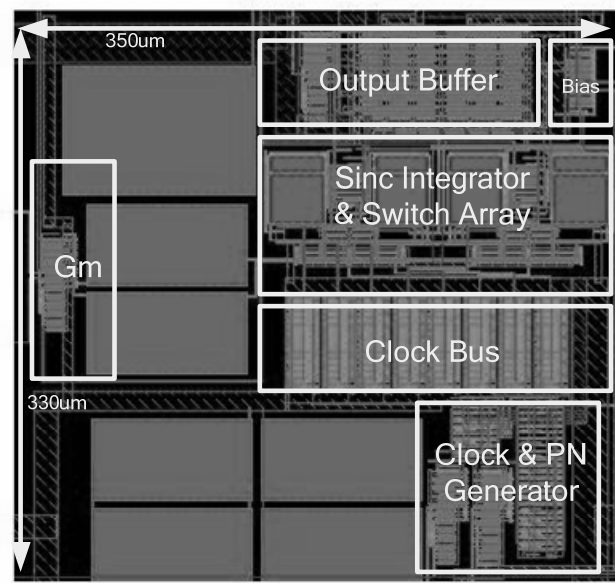


Fig. 6.7 Layout of a single path in IBM 90 nm CMOS

## 6.2 System level simulation and signal reconstructions

Block level simulations suggest a SNR above 44 dB. However, the signal needs to be reconstructed from the simulated outputs of the front-end in Cadence to confirm the achievable reconstructed signal quality. Theoretically speaking, once we know the PN sequences that we employed, we can easily use the algorithm provided in Chapter II to reconstruct the incoming signals. The PN sequences are generated by known digital circuits so we know what exactly the binary sequences we sent to the mixers. However, In fact we don't really know the actual PN sequences applied in the real circuit, because they are distorted by many kinds of circuit non-idealities. A few examples are shown as below.

## a) Charge leakage

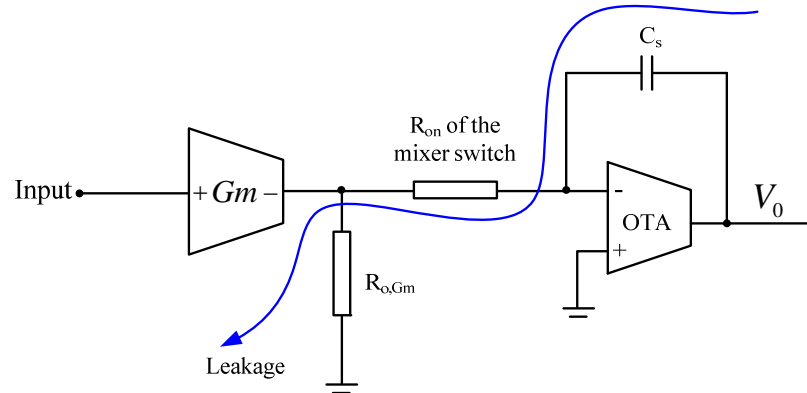


Fig.6.8 Illustration of a single path circuit

The simplified schematic of a single path is shown in Fig.6.8. The integrated signal charge in the sampling capacitor  $C_s$  keeps leaking exponentially through the finite output resistance of the  $G_m$  stage, denoted as  $R_{o,Gm}$ . The time constant is given by  $\tau = AR_{o,Gm}C_s$ , where  $A$  is the DC gain of the OTA. Due to the leakage, signal amplitude at the beginning of the sampling window is attenuated and the realistic sampling window is approximated as shown in Fig. 6.9. The amplitude of the real PN sequence is shaped by the sampling window, introducing signal errors.

## b) Clock offset

The sampling clock generator and the PN generator are fed by a master clock signal however the master clock signal goes across the whole circuit chip so it arrives at different digital circuit blocks at different instants. The sampling window of each single



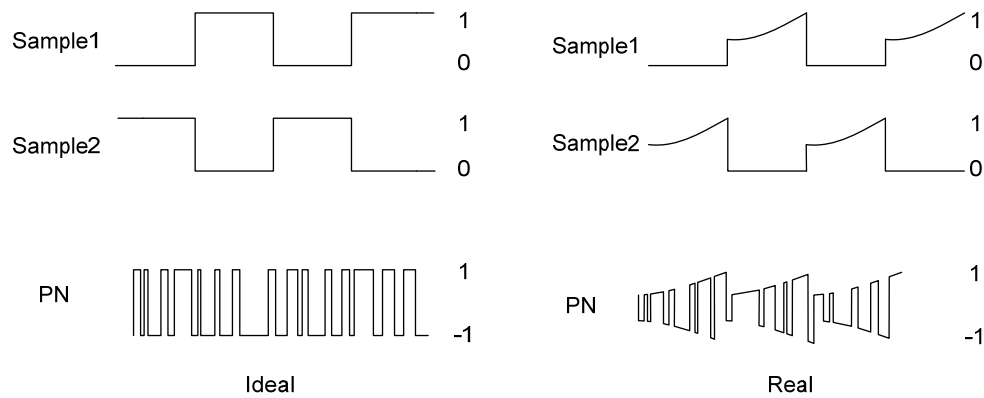


Fig. 6.9 Ideal and real sampling windows and PN sequence

path is shifted by this timing-offset. After the mixer, the signal is randomized so it consists of significant high frequency component. When high frequency signal is sampled, very little timing-offset of the sampling window will create considerable signal error.

c) Finite rising / falling time and clock feed-throughs

In reality, finite rising and falling time, as well as clock feed-throughs will further distort the PN sequence (Fig. 6.10).

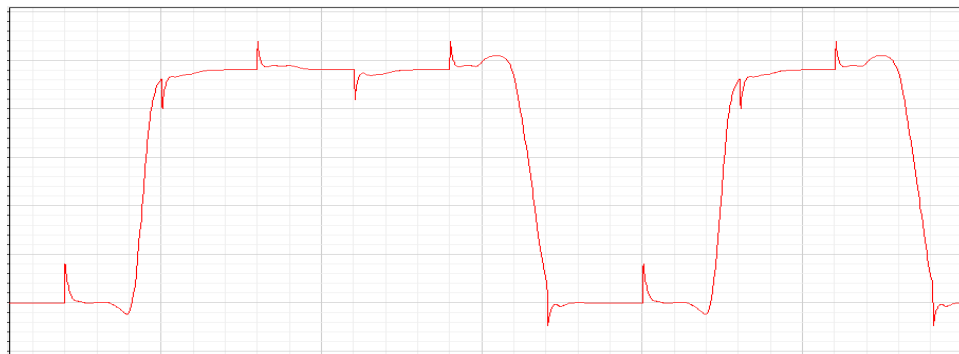


Fig. 6.10 The PN sequence with finite rising/falling time and clock feed-throughs

In order to show the effect of circuit imperfections on the signal reconstruction quality, a series of simulations have been conducted. In the simulation, the input signal to the front-end is assumed to be a *16-sparse* frequency-domain multi-carrier signal with 128 subcarriers, i.e.  $S = 128$  and  $K = 16$ . The subcarrier-spacing  $\Delta f = 1\text{GHz}/128 = 7.8125\text{MHz}$  and the symbol duration time  $T = 1/\Delta f = 128\text{ns}$ . The location of the 16 active subcarriers are chosen randomly and changed every  $T$  seconds.

Fig.6.11 gives the MSE (Mean Square Error) of the reconstructed signal versus the NSR (Normalized Sampling Rate) when there is no circuit imperfection. As shown, the MSE is around -200dB when the NSR is increased up to around 0.5, which means that the signal can be viewed as reconstructed perfectly when the sampling rate goes beyond half of the Nyquist rate.

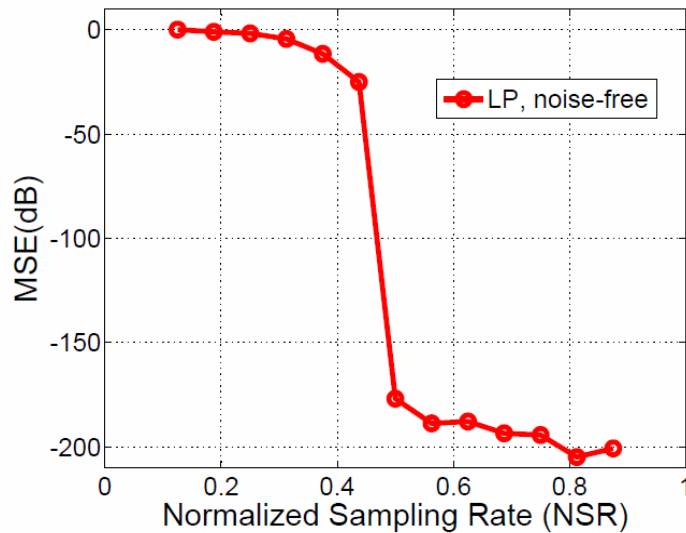


Fig. 6.11 MSE of the reconstructed signal versus the normalized sampling rate when there is no imperfection

Fig. 6.12 shows the MSE of the reconstructed signal when the PN sequences have finite settling time, from these figures, we can see the system performance degrades if the circuit non-ideal factors are not treated properly. For example, with a finite settling time of 30ps, the best achieved MSE is only -20dB.

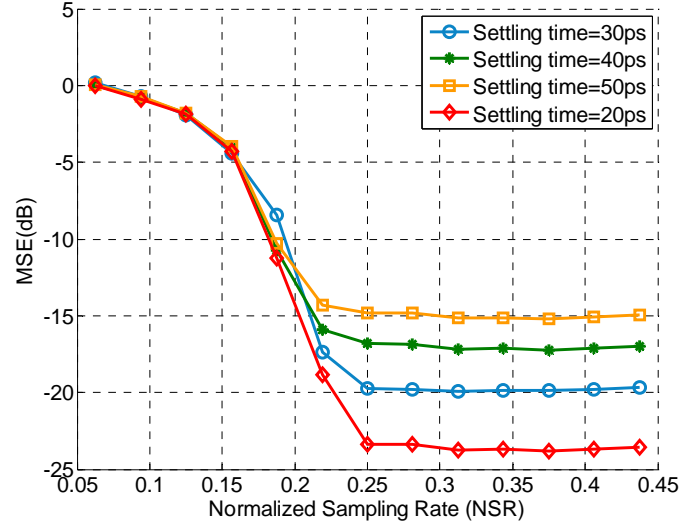


Fig. 6.12 MSE of the reconstructed signal versus the normalized sampling rate when the random PN sequences have finite settling time

Calibrating those high order errors in post digital domain is difficult. However, fortunately the circuit non-idealities shown above are static errors and may be calibrated by the training technique shown in Fig.6.13.

In Fig.6.13,  $y$  is the spectrum of the input signal and  $S$  is the sampled measurements.  $V+\Delta V$  is the distorted  $\Phi\psi^H$  that contains all the linear static non-idealities  $\Delta V$  in the circuit. Size of  $V+\Delta V$  is  $M*N$ , where  $N$  is the length of  $y$ , which is equal to the number of overall carriers in our case, and  $M$  is number of the overall

sampled measurements for each input carrier, depending on the expression  $K \log_2(N/K)$  in section II. When every known single carrier signal is transmitted through the receiver, the output  $S$  is actually the single column of  $V + \Delta V$ . The whole  $V + \Delta V$  can be measured by transmitting all  $N(256)$  carriers through the receiver. In other words the number of calibration iterations is equal to the number of sub-carriers  $N$ . The time that we need to transmit a single carrier needs to be integral multiples of periods of all carriers so it is  $1/\Delta_f$ , where  $\Delta_f$  is the minimum frequency spacing among those  $N$  carriers.

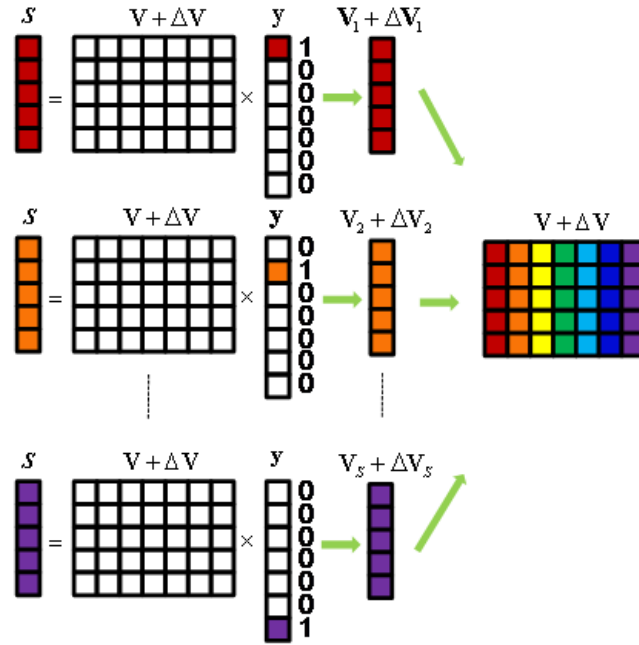


Fig. 6.13 Illustration of the direct training approach to deal with the circuit imperfections

Validating the direct training approach with circuit level simulations is very time-consuming (several months of simulations). The reason is that in the system there are

both high frequency sources such as the PN sequence and low frequency signal such as the compressed output signal. High frequency signal makes the timing step for transient simulation very small and low frequency output can only be measured if used a very long time window. Due to the signal compression, the required time window for our simulation is extremely long compared to the timing step. As explained above, the proposed calibration process requires transmitting all carriers one by one through the receiver, this requires several simulation months to get the reconstruction matrix  $V$  via simulation. Though it is impossible to simulate the entire matrix  $V$  of the proposed carriers' base, validating the training technique with fewer carriers can be done within a few weeks. Here special simplified input signal with smaller carrier bases are employed to simulate the reconstructed signal quality through direct training, for making the simulation time reasonable.

Assume we have 20 tones normally distributed over bandwidth of 0~1GHz. Only 2 tones among them are active. The spectral occupancy (sparsity) is 10%. According to Fig.2.4, the required sampling rate is 46%. In simulation the receiver's sampling speed is adjusted to 46% of the Nyquist rate which is 2GHz. The speed of the PN sequence is also dropped to 2GHz in order to increase the simulation time step. We ran coarse transient simulation 20 times to get the reconstruction matrix  $V$ , then we transmit a two-tone signal through the receiver, finally we are able to reconstruct the original two-tone input with a SNDR around 40 dB. An example of the reconstructed spectrum is shown in Fig.6.14.

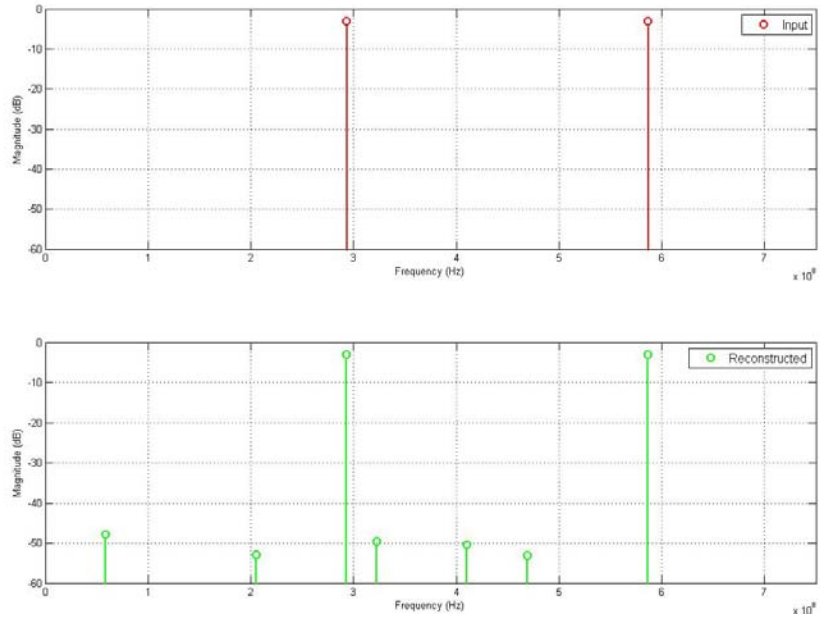


Fig.6.14 The reconstructed signal spectrum through directly training with coarse transient simulations

Note that accurate conservative transient simulation takes too long time so coarse simulation setup were used. Though the result is not accurate, the reconstructed SNDR is close to what the block level simulations expect.

The proposed receiver can be compared to a stand alone 3 GS/s and 44 dB SNDR ADC. Such a high speed and medium resolution ADC can be implemented employing a time-interleaved ADC architecture. Some recently published high speed time-interleaved ADCs are listed in Table 6.3. A flash ADC [29] is also included in the table. The Figure of Merit (FOM) is defined as the consumed energy per conversion step. When the signal is sparse, the FOM of the proposed receiver is significantly better due to the power reduction.

Table 6.3 Performance overview of comparable stand alone ADCs

Design	[5]	[6]	[7]a	[7]b	[29]	This work (sim.)
Sampling Rate (GS/s)	1	0.8	1.35	1.8	3.5	3
ENOB (SNDR in dB)	8.85 (55)	9 (56)	7.7 (48.2)	7.9 (49.4)	4.9 (31.18)	7 (44)
Power consumption (mW)	250	350	180	420	98	120.8
Process(nm)	130	90	130	130	90	90
FOM (pJ/conversion step)	0.56	0.85	0.64	0.98	0.94	0.31
Signal Sparsity	Arbitrary					4%

$$FOM = \frac{P}{2^{ENOB} SR},$$

where  $P$  is the power and  $SR$  is the ADC sampling rate.

The power consumption of the digital PN and clock generators is as high as 62% of the overall power in the proposed RF front-end, which will shrink significantly with technology scaling. In table 6.3, only the ADC core power is considered. A finer comparison that takes into account the power consumption of the master clock generating circuit (such as the Phase Lock Loop) is provided in Chapter VII.

The sampling rate of the integrator and the sampler only depend on the clocking scheme, leading to a flexible reconfigurability that enables the system to accommodate input signals with different sparsity levels. Although the system designed in this Chapter targets a signal sparsity of around 4%, by over-designing the OTAs and ADCs, the sampling rate of the system can be increased up to the Nyquist rate to sample non-sparse signals. As shown in Fig. 2.4, when an input signal exhibits a high degree of sparsity, the required system sampling rate is low and signals are readily reconstructed with a CS algorithm. When the signal sparsity is 25% or larger, the required sampling rate approximates the Nyquist rate and the Least Square (LS) algorithm may be used to reconstruct the signal [30]. The LS algorithm is able to reconstruct signals with arbitrary sparsity when the system works at Nyquist rate. The OTA needs a *GBW* of 600 MHz to settle within 7 bits resolution. Furthermore, the sampling rate of the following ADCs needs to be tunable up to 380 MS/s.



## CHAPTER VII

### TESTING OF THE CS DATA ACQUISITION SYSTEM

#### 7.1 The testing with discrete components

Before the testing of the integrated front-end designed in chapter VI and fabricated with IBM 90nm CMOS process, a CS system implemented with discrete components and microcontrollers was built and tested for the purpose of prove of concept. Discrete components have different characteristics from the integrated circuits so the front-end topology is a little bit different from what is proposed in Chapter III. For example, the Gm stages implemented by discrete amplifiers have very large output resistance and fairly good linearity due to large supply voltages so active integrators are not necessary and only passive integrators are employed. Furthermore, sampling windows of two integrator branches overlap at their edges for providing the flexibility on setting the locations of the nulls of the sinc type LPF [28].

The simplified math model of the system is shown in Fig.7.1. The math model is a little bit different from that introduced in Chapter II because of the overlapping sampling window so the variables mentioned in this section are clarified as follows. The received signal  $r(t)$  is the transmitted frequency-domain K-sparse real signal  $x(t)$  plus the additive white noise. For the time period of  $t \in [0, T]$ , the received signal is sent to the proposed  $N$ -path receiver. At the  $ith$  path, the received signal is mixed with a local

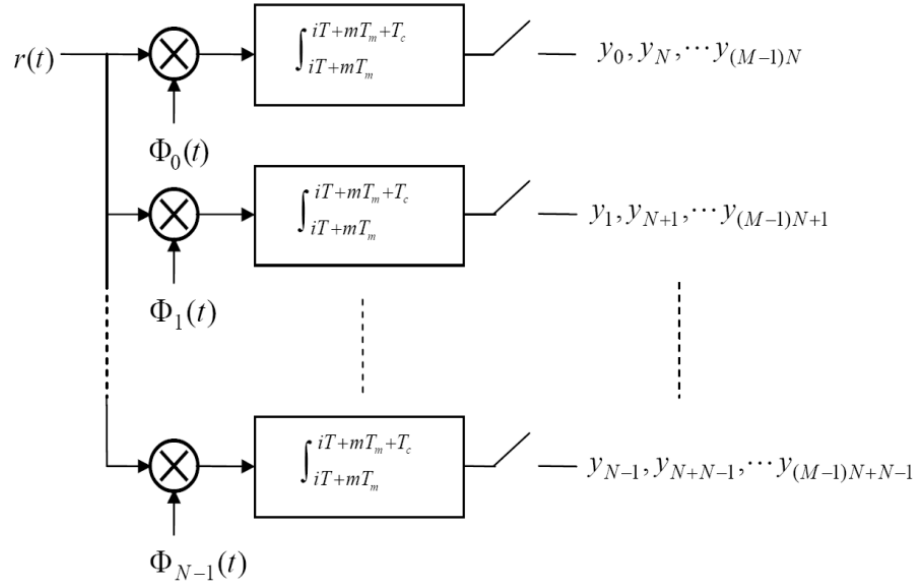


Fig.7.1 System architecture

random signal  $\Phi_i(t)$  and the output of the mixer is sent to an integrator. The integrator has an integration duration of  $T_c$  which is a segment of  $T$ . Moreover, two adjacent integration periods have an overlapping time of  $T_c - T_m$ . The output of the integrator is read out and the integrator is reset every  $T_m$  seconds (Note: the first read and reset operations happen after  $T_c$  seconds).

Alternatively, the above mixer and integration procedure can be viewed as the received signal  $r(t)$  is segmented into  $M$  pieces  $r_m(t) = r(t)w_m(t)|_{m=0}^{M-1}$  with a duration time  $T_c$  and overlapping period  $T_c - T_m$ , where,  $w_m(t)$  is the windowing function, and then the time windowed signal  $r_m(t)$  is sent to the integrator with a integration period of  $T$ .

Since each path produces  $M$  samples, there are total  $L = MN$  samples generated every  $T$  seconds and the  $m_{th}$  measurement of the  $n_{th}$  branch is given by:

$$y_{mN+n} = \langle r_m(t), \Phi_{mN+n}(t) \rangle = \int_0^T r_m(t) \Phi_n^*(t) dt \int_{mT_m}^{mT_m + T_c} r(t) \Phi_{mN+n}^*(t) dt \quad (7.1)$$

Where,  $\Phi_{mN+n}(t) = \Phi_n(t)w_m(t)$  is chosen randomly for all  $m$  and  $n$ .

In the back-end of the receiver, the total  $L = MN$  samples are processed together using the Orthogonal Matching Pursuit (OMP) to reconstruct the transmitted signal.

#### a) Parameter setting

In the built prototype, the input signal is a BPSK modulated multi-tone sparse signal with a bandwidth of 200 KHz, the transceiver consists of 4 parallel paths working at 32 KHz, which means that each path works at only 8% of the Nyquist rate and the whole receiver works at 32% of the Nyquist rate. The input signal is assumed to be a 4-tone BPSK modulated multi-carrier signal which range over the frequencies of 0~200 KHz. The channel spacing is 2 KHz. The complete testing period is 500 $\mu$ s so all the channels have integral number of periods during the testing period. Matlab simulation shows that the system can achieve a BER(Bit Error Rate) of 5.36E-4 when each parallel path produces 16 samples over 500 $\mu$ s, i.e.,  $M = 16$ . The Gm stages are implemented with TIOPA861 that provides 116 mS transconductance gain. The switches are implemented with discrete transmission gates CD4066BCN. The sampling capacitor is 17 nF.  $T_c$  is 36.5  $\mu$ s and  $T_{OV}$  is 5.6  $\mu$ s.

b) The implementation of the Test-bed and building blocks

The overall configuration of the test-bed is shown in Fig.7.2, where the digital part is responsible for generating the input sparse signal, the triggering signal, the pseudo-random basis and the clock. The analog part is used to realize the random basis projection that is essential for the signal reconstruction. The build-in ADC in the oscilloscope is used to collect the sampled data. Then, the collected data is sent to PC and processed by Matlab code to reconstruct the signal.

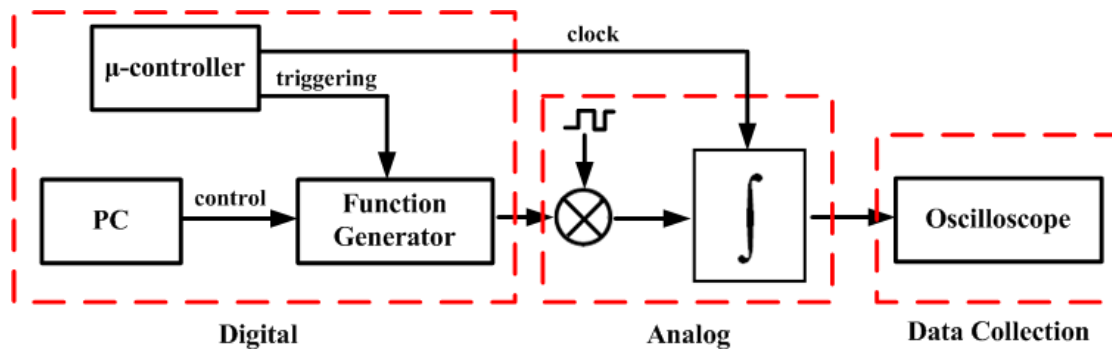


Fig.7.2 Overall configuration of the test-bed

Agilent 33120A arbitrary waveform generator is used to generate the input multi-tone sparse signal. The output port of the generator is triggered by the micro-controller in order to synchronize with the integrator clock that is also generated by the micro controller. Fig. 7.3 gives an example of a five-tone signal which consists of carriers at 2 kHz, 8 kHz, 10 kHz, 16 kHz and 18 kHz. Fig. 7.4 shows the actually photo shot of an example of the generated multi-tone waveforms.

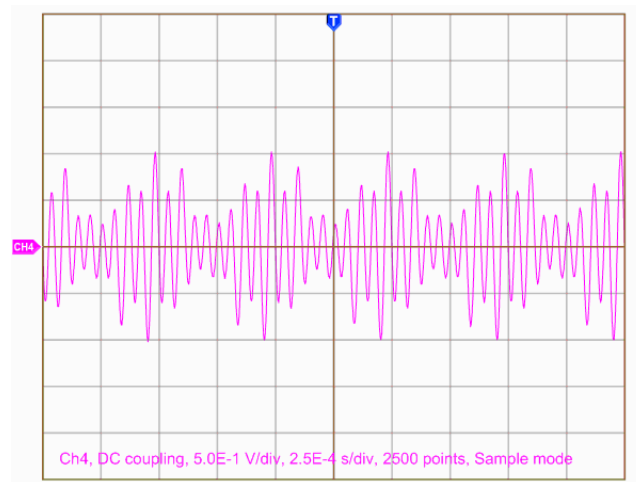


Fig.7.3 Multi-tone signal with frequencies 2kHz, 8kHz, 10kHz, 16kHz, 18kHz

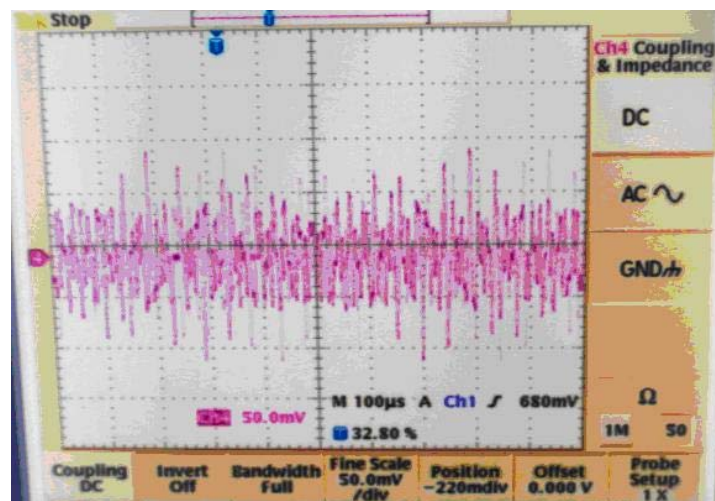


Fig. 7.4 The photo shot of the generated multi-tone waveforms

The integrator schematic is shown in Fig.7.5.

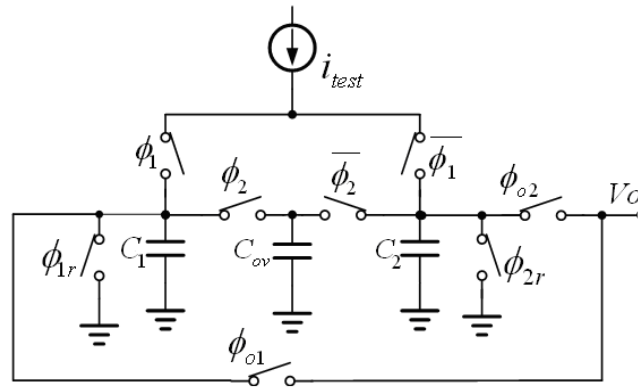


Fig.7.5 Schematic of the integrator with overlapping windowing

$\phi_1$  and  $\bar{\phi}_1$  are two integration switches for the left and right branches, respectively.  $\phi_{o1}$  and  $\phi_{o2}$  are readout switches;  $\phi_{1r}$ ,  $\phi_{2r}$  are reset switches. The clock diagram is shown in Fig.7.6.

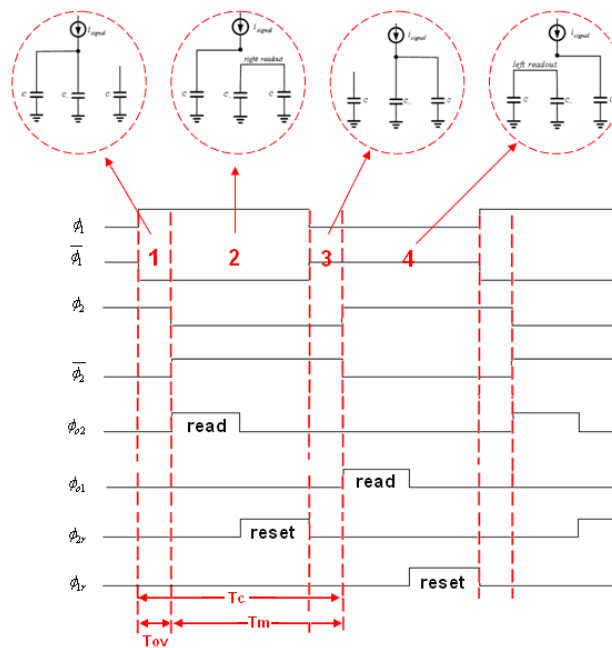


Fig.7.6 Clock diagram of the integrator

As shown in Fig.7.6, phase<sub>1</sub> and phase<sub>3</sub> are two overlapping durations, phase<sub>2</sub> and phase<sub>4</sub> are readout phases for the right and left branches, respectively. The equivalent integration windows are shown in Fig.7.7.

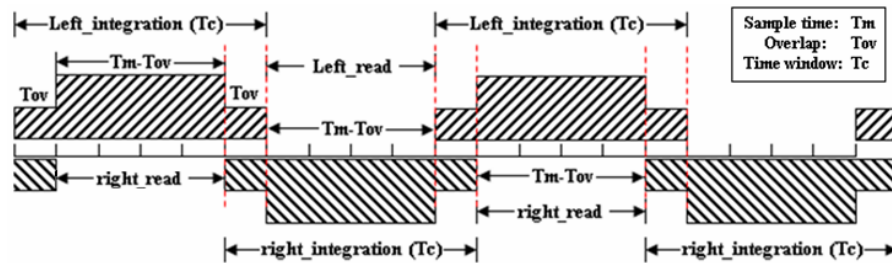


Fig.7.7 Time window of the integrator

The complete circuit implementation for a single path is shown below in Fig.7.8.

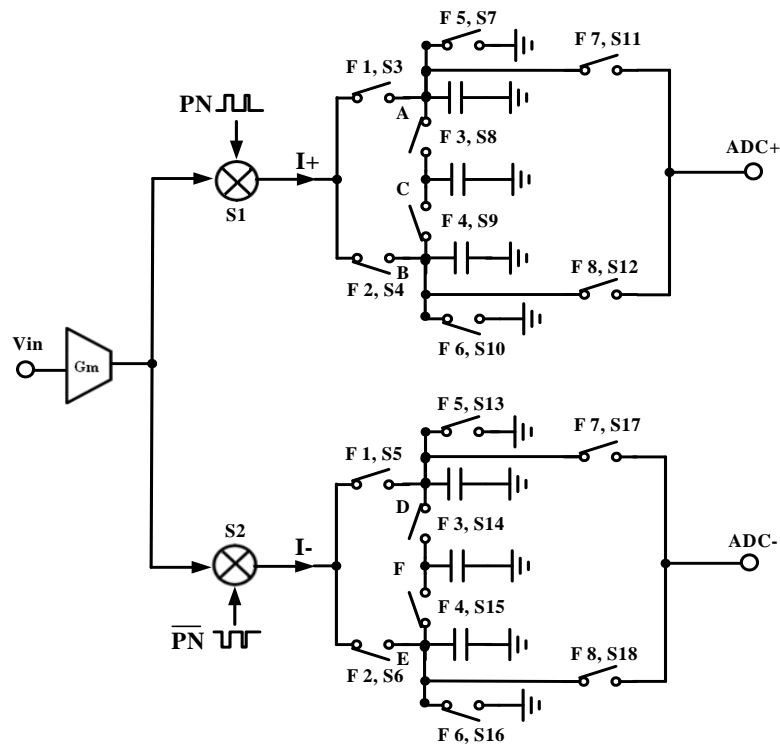


Fig. 7.8 The circuits implementation for a single path

At each path, the mixer consists of transmission-gate switches controlled by PN sequences. The PN sequence is implemented with a linear feedback shift register (LFSR). In our prototype, the clock frequency is chosen to be 1 MHz, which is higher than the Nyquist sampling rate. There are 4 parallel paths and 4 independent PN sequences with a length of 500 are needed. An 11-bit LFSR is used to generate a PN sequence with a length of 2047 and then divided into 4 segments.

The inherent ADC of the oscilloscope (Tectronix TDS 3054 500MHz, 5Gs/s) samples the output of the integrators. The sampled data is transferred to the PC via the GBIP port.

The signal is reconstructed in Matlab through the Orthogonal Matching Pursuit by exploiting the direct training method introduced in Changer VI. 100 single-tone training symbols are first sent to form the 64 by 100 reconstruction matrix. Then, the system is tested with multi-carrier data symbols:  $r(t) = \sum_i a_i \cos 2\pi f_i t$ , where  $a_i = +1$  or  $-1$ ,  $f_i = (2 * i - 1) \text{ KHz}$  ( $i = 1, 2, \dots, 100$ ). Some reconstructed examples are shown in Table 7.1, where the signal is expressed as a vector of its frequency components with the negative sign representing the BPSK modulated information of “-1”. The frequencies and their modulated phases are correctly reconstructed. The system can reconstruct multi-tones signal with number of tones up to 4. The photo shot of the complete test bench is shown in Fig.7.9. The employed print circuit board is shown in Fig.7.10. The actual generated clock signals that control the integrators are shown in Fig.7.11. An example of the final output waveform exiting the integrator is given in Fig.7.12. In



Fig.7.12 it is shown that during the reading and holding phases the waveform is not flat, it is because of the leakage current from the sampling capacitor. Though it is difficult to avoid leakage current with discrete circuit parts, this problem is later solved with the integrated front-end where the leakage current is comparably small.

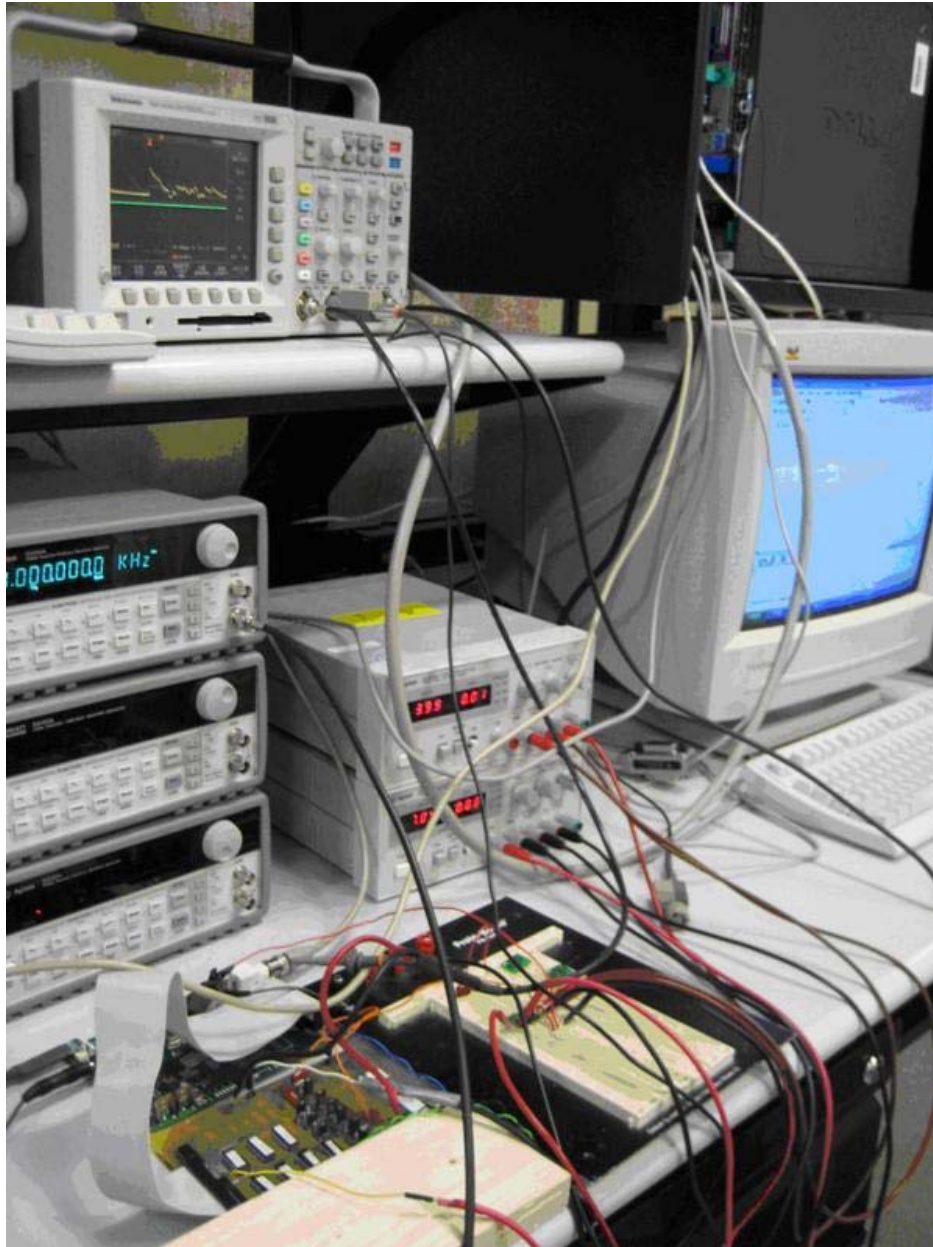


Fig.7.9 The whole test bench setup

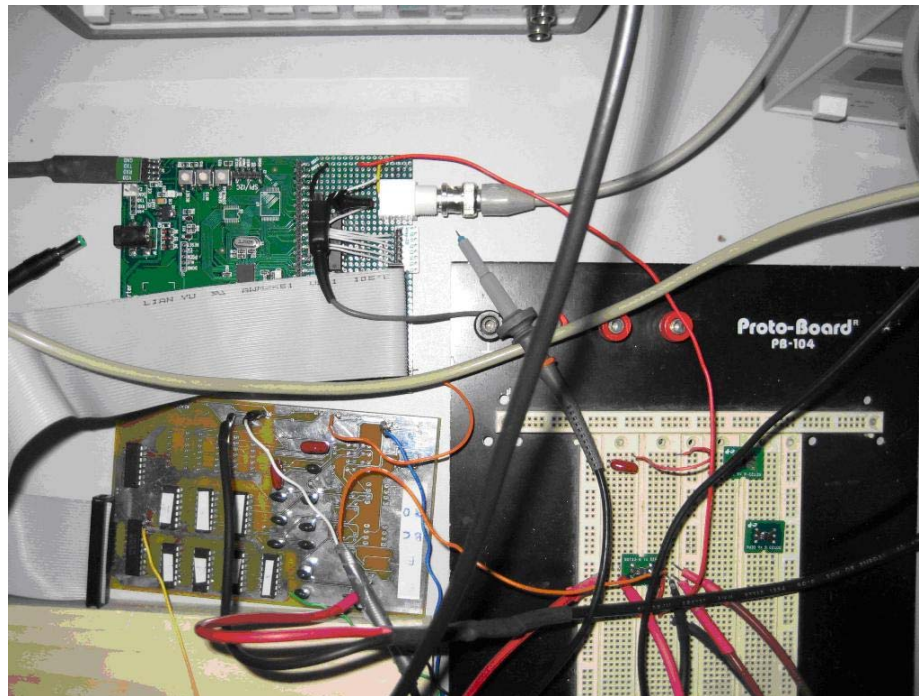


Fig. 7.10 View of the circuit board

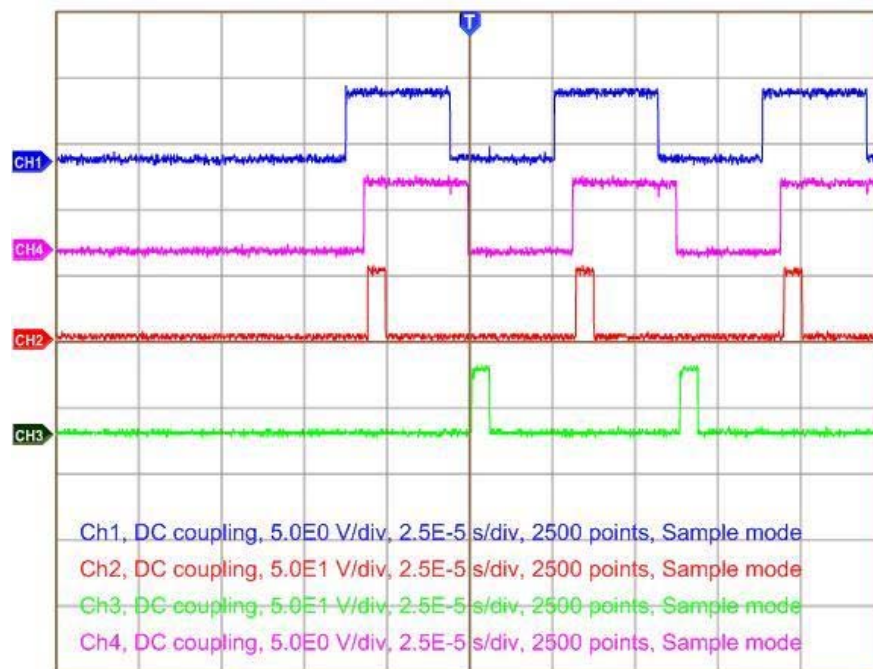


Fig.7.11 System clocks generated by the microcontroller

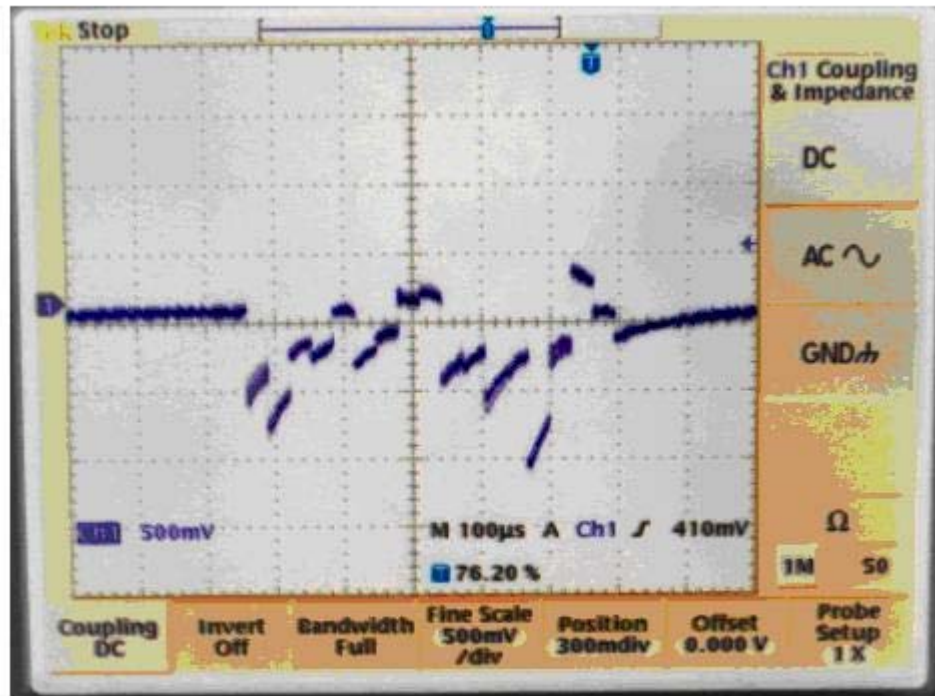


Fig. 7.12 An example of the waveform at the output of a single path

Table 7.1 Measurement results

Sub-carrier's amplitude (mV)	Input Testing signal frequency (kHz)	Reconstructed signal's frequency (kHz)
0.3	[61, 121]	[61, 121]
0.3	[41, 131]	[41, 131]
0.3	[41, -131]	[41, -131]
0.3	[-51, 63, 111]	[-51, 63, 111]
0.2	[71, -85, 91, -101]	[71, -85, 91, -101]

## 7.2 An IC front-end fabricated with 90nm CMOS process

### a) Introduction

The CS front-end designed in Chapter VI is fabricated with IBM 90nm CMOS process. The on-chip system contains one single path including the Gm stage, the differential mixer, the active integrator, the sampling clock generator and the PN generator. Some auxiliary circuit blocks such as the biasing current generator, the clock buffers and the output testing buffers are also included. The complete 8 paths CS system may be implemented on a single print circuit board incorporated with 8 individual fabricated chips. In chapter VI the system is originally designed for accommodating wide band input signal from 0~1.5GHz. In this chapter, the arbitrary wave generator agilent N8241A which is employed in the testing to generate the wide band multi-tone signal provides a maximum signal bandwidth of 500 MHz, so the input bandwidth is 0~500 MHz in the testing. The internal clock of the arbitrary signal generator is 1.25 GHz, which is used as the master clock of the PN generator.

The input is assumed to be a multi-tone BPSK signal. The frequency spacing between adjacent carriers is assumed 5 MHz. The 100 carriers' base is from 5MHz to 500MHz. It is also assumed that the frequency domain sparsity of the input signal is around 4%, which means that there are at most 4 active tones. The minimum required data rate of the PN sequence needs to be as high as the Nyquist rate, which is 1 GHz. In our test bench, the speed of the PN generators is 1.25 GHz. According to Fig.2.4, the minimum required sampling rate is 26% of the Nyquist rate. In the testing, we set the

system sampling rate conservatively at 36%, which is 360 MS/s. Since 8 paths are employed to form the whole CS system, each path samples at 45 MHz.

The time duration of a single testing run is  $1 / 5 \text{ MHz} = 200 \text{ ns}$  so that it is the integral multiples of the all carriers' periods. The employed PN generator contains 11 flip-flops and generates a PN sequence with overall length of 2047. The length of each PN sequence in a single path is about 256, with a time during of  $256/1.25=204.8 \text{ ns}$  which is sufficient to cover the complete testing duration. The input signal power is assumed -20 dBm referred to 50 ohm. The system level specifications of the CS system in the testing are provided in Table 7.2.

Table 7.2 Design specs of the CS front-end in testing

Input Signal Bandwidth	5 MHz ~ 500MHz
Number of Parallel Paths	8
Single Path sampling rate (10/256 signal sparsity)	45 Ms/s
Overall System Sampling rate	360 MS/s (36% Nyquist Rate)
Fullscale input / output	-20 dBm / -2 dBm (referred to 50 ohms)

b) The testing setup

At the beginning of the testing run, the 8 PN sequence generators in the 8 paths need to be reset to the required initial states for generating different uncorrelated PN sequences. The suggested initial states for the 8 PN generators are listed in Table 7.3. QN represents the output state of the Qth flip-flop.

Table 7.3 Initial conditions for 8 independent PN sequences

	Q 1	Q 2	Q 3	Q 4	Q 5	Q 6	Q 7	Q 8	Q 9	Q 10	Q 11
PN1	1	1	1	1	1	1	1	1	1	1	1
PN2	1	1	1	0	1	0	1	0	1	1	0
PN3	0	0	0	0	0	0	1	0	1	0	1
PN4	1	1	1	1	0	1	0	1	0	0	1
PN5	0	0	1	0	1	0	1	1	0	0	0
PN6	0	0	1	0	1	0	1	0	0	1	0
PN7	1	1	0	1	0	0	0	0	1	1	0
PN8	1	1	1	0	1	1	1	1	0	0	1

In this chapter, one single path is re-used to emulate the behavior of the 8 paths system for lowering testing cost. The data sampled in the first 200 ns are considered as the data from the first path. The single testing duration 200 ns is the integral multiples of any carrier's period, so the wideband input signal repeats again from 200 ns to 400 ns and the tested path emulates the operation of the second virtue path. In this time period, the PN sequence is un-correlated with the PN sequence's first section from 0 ns to 200 ns, and the data sampled from 200 ns to 400 ns are considered as the data sampled from

the second path. In the same way, the tested path emulates the third path from 400 ns to 600 ns. The testing duration lasts for 1600 ns to get sampled data of all the 8 paths. The test bench diagram is shown in Fig.7.13. A photo copy of the test bench is shown in Fig.7.14. The ADC is emulated by the digital oscilloscope DSA91304A. The differential front-end outputs are sent to the oscilloscope by the differential probe 1169A. The clock signals, triggering signals, as well as the arbitrary wideband tested signal, are all generated by the arbitrary waveform generator N8241A so they are readily synchronized and phased locked inside the N8241A. The jitter variance of the 1.25 GHz clock signal provided by N8241A is 4.13 ps, so the proposed system targets for SNR of 41 dB according to equation (4.6).

On the PCB, RF transformers cx2156 with bandwidth 2.3MHz~2700MHz turn the single-ended arbitrary input signal and the single-ended clock signals into differential signals. Differential signals are sent into the one-path chip for rejecting common mode noises. Furthermore, due to the bondwire inductance, the GND inside the chip and the GND on the PCB are not exactly the same. The mismatches between the board GND and the chip GND are also rejected when differential clocks are sent. Biasing voltages and currents are controlled by potentiometers. The photo copy of the PCB is shown in Fig.7.15.







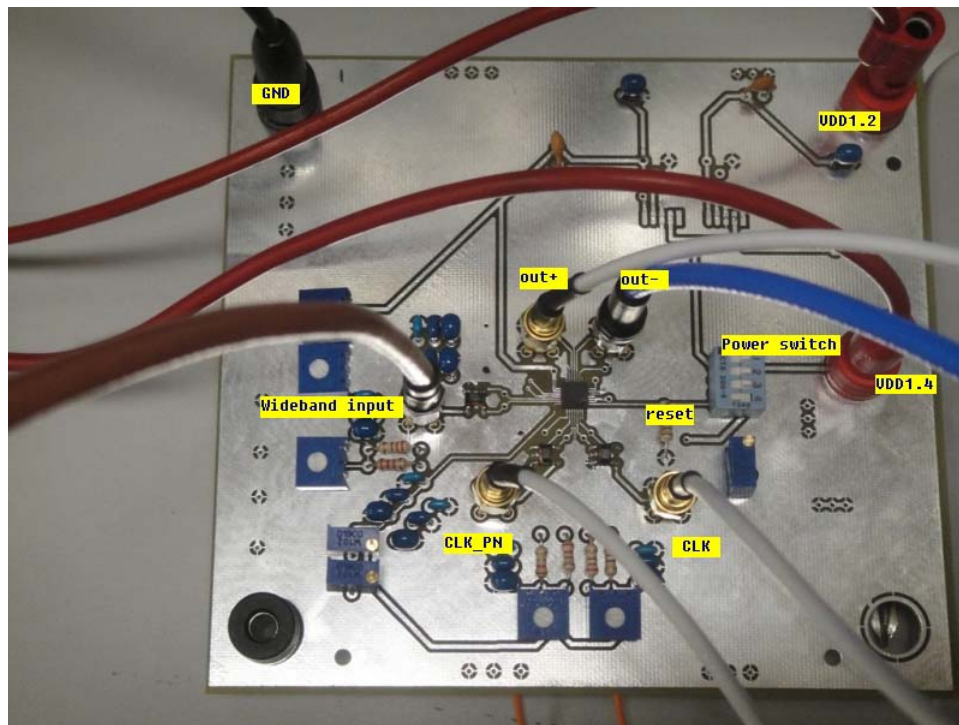


Fig.7.15 The photo copy of the PCB

c) The testing result and the signal reconstruction

An example of the output wave is shown in Fig.7.16. Each path needs to obtain  $200 \text{ ns} * 45 \text{ MHz} = 9$  samples. When one single path is reused, overall 72 samples are obtained at the output. The green waveform is the reset/trigger signal that synchronizes the starting point of the PN sequence and the phase of the input carrier signal. The enlarged waveform is shown in Fig.7.17, with the reading and resetting phase marked.

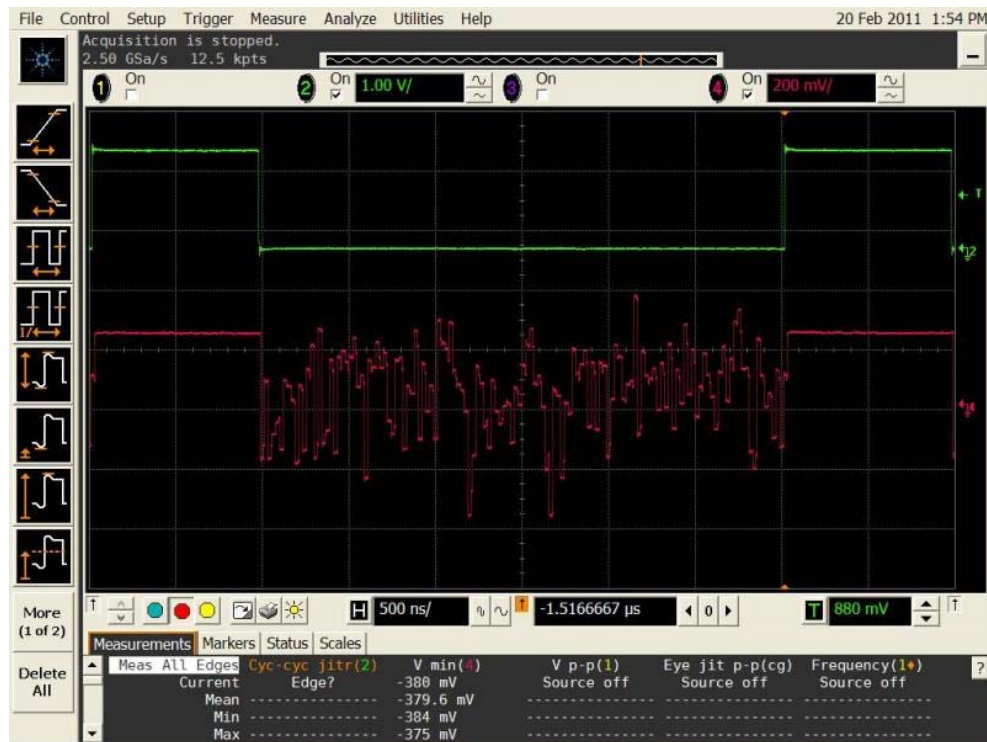


Fig.7.16 The screen shot of an example of the output waveforms (50MHz input)

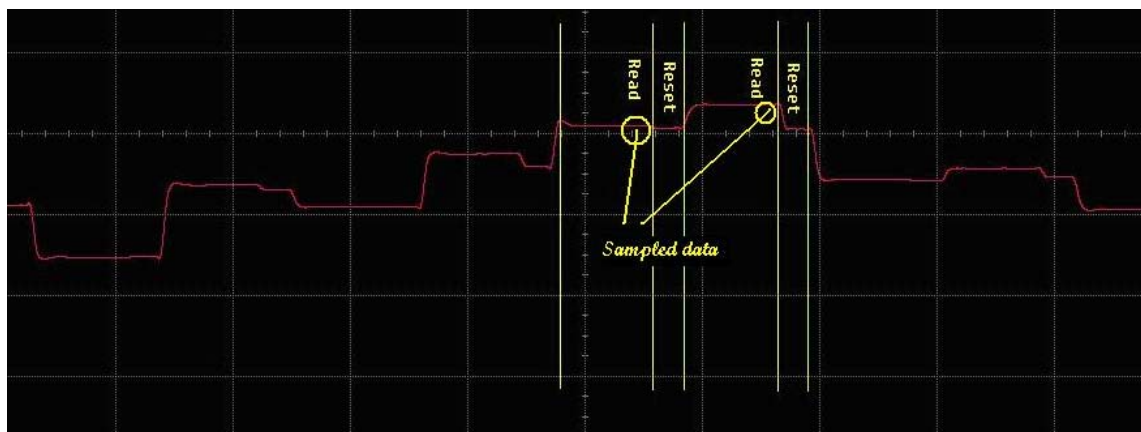


Fig.7.17 Illustration of the reading and resetting phase (a piece of the output waveform with 50MHz input)

Sampled data that are distributed to 8 paths are illustrated in Fig.7.18.

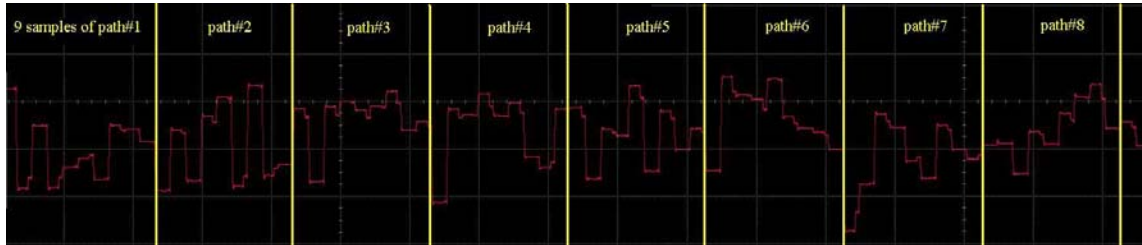


Fig.7.18 The reusing of a single path to get sampled data from 8 paths

Direct training is employed to reconstruct the input signal in digital domain. Each tone is transmitted through the front-end and the output vectors are measured and stored to form the reconstruction matrix. If the input signal has arbitrary phases, both sin waves and cosine waves of all the carrier frequencies need to be trained to obtain the complete reconstruction matrix that associates both sin and cosine carriers' base. In the proposed prototype the BPSK signal is present at the input and the phases of the desired signals are either 0 or 180 degree. Thus only sine waves of the carrier frequencies need to be trained to reconstruct the assumed BPSK signal. If the input signal is a QPSK signal or signals with arbitrary starting phases, the cosine waves at carrier frequencies also need to be trained.

With the measured reconstruction matrix, arbitrary wideband BPSK input signals over 5MHz~500MHz frequency range with a frequency domain sparsity of 4% or less can be reconstructed. We defined the reconstructed signal SNR as the overall power at the desired signal carriers over noise power over all other undesired frequency spectrum

(overall integrated power of the noise floor). The SNR obtained in the single tone test over the band of interest is shown in Fig.7.19.

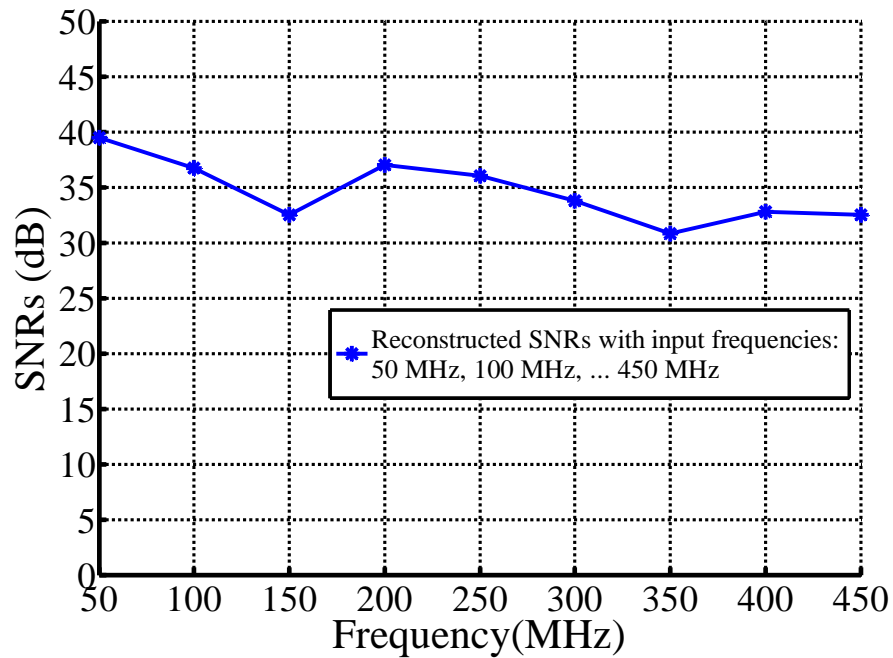


Fig.7.19 The reconstructed SNR vs. frequency

Some reconstructed spectrums obtained with multi-tones input signals are shown as belows. The reconstructed SNRs are between 24 dB and 30 dB. The Spectrums of case 1~5 are plotted with absolute values. The spectrum of case 6 is plotted with the original amplitude including the negative signs.

Case 1:

Freq=20MHz, 70MHz, 250MHz, 450MHz

The reconstructed SNR= 27.74dB

The reconstructed spectrum is shown in Fig.7.20.

Case 2:

Freq=50MHz, 250MHz, 490MHz

The reconstructed SNR=29.2627dB

The reconstructed spectrum is shown in Fig.7.21.

Case 3:

Freq=50MHz, 150MHz, 250MHz, 490MHz

The reconstructed SNR= 29.42 dB

The reconstructed spectrum is shown in Fig.7.22.

Case 4:

Freq=50MHz, 250MHz, -490MHz (with 180 degree initial phase)

The reconstructed SNR= 29.616 dB

The reconstructed spectrum is shown in Fig.7.23. The plotted amplitudes are the absolute values.

Case 5:

Freq=20MHz, -70MHz (with 180 degree initial phase), 250MHz, 450MHz

The reconstructed SNR= 26.657 dB

The reconstructed spectrum is shown in Fig.7.24. The plotted amplitudes are the absolute values.

Case 6:

Freq= -20MHz (with 180 degree initial phase), -70MHz (with 180 degree initial phase),  
250MHz, 450MHz

The reconstructed SNR= 24.53 dB

The reconstructed spectrum is shown in Fig.7.25.

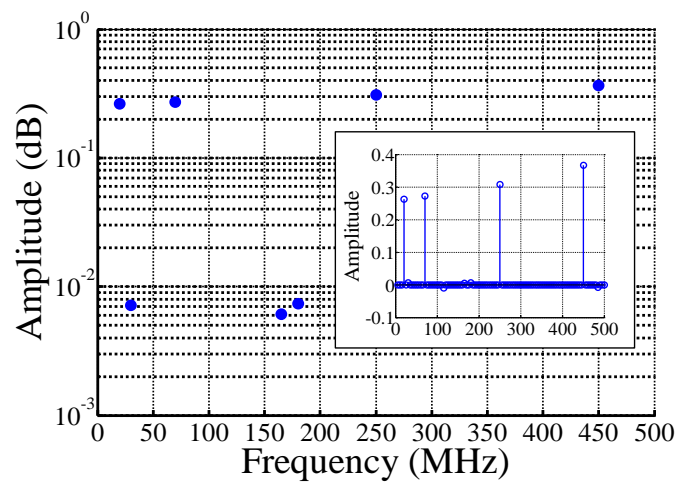


Fig.7.20 The reconstructed spectrum with the input at 20M, 70M, 250MHz, 450M

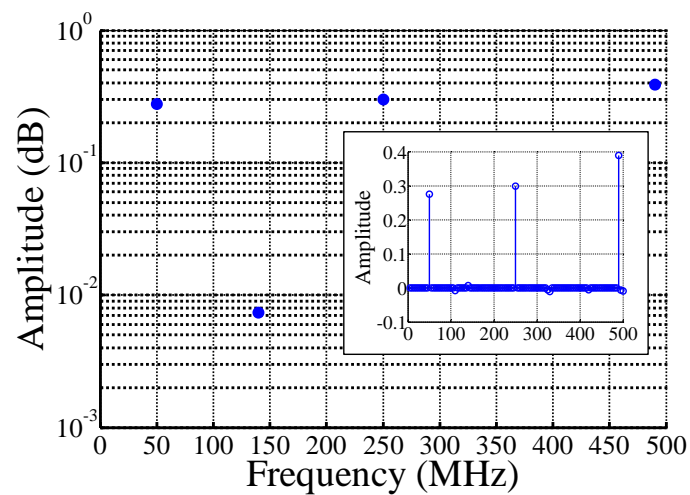


Fig.7.21 The reconstructed spectrum with the input at 50M, 250M, 490M

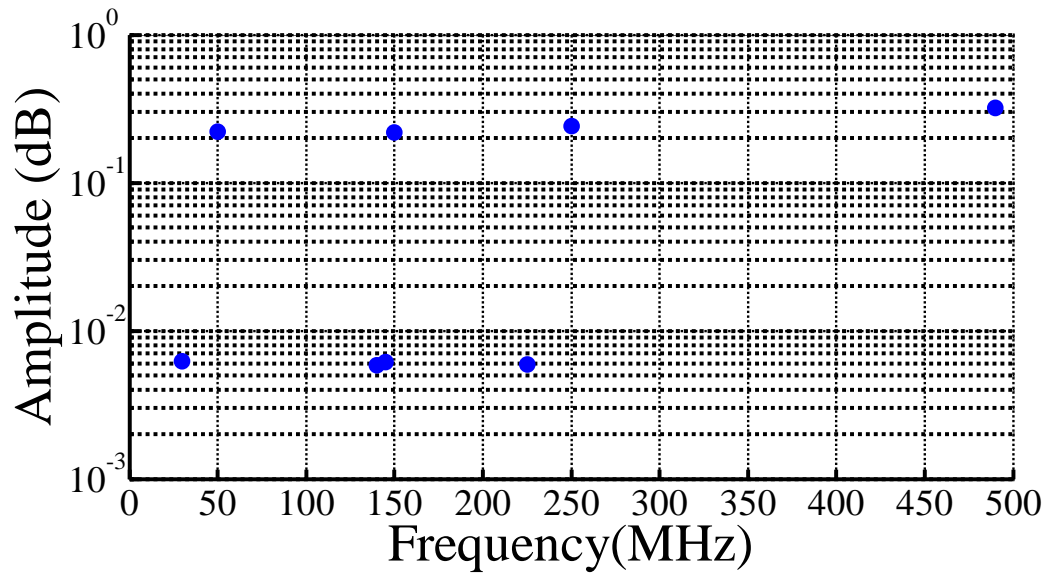


Fig.7.22 The reconstructed spectrum with the input at 50M, 150M, 250M, 490M

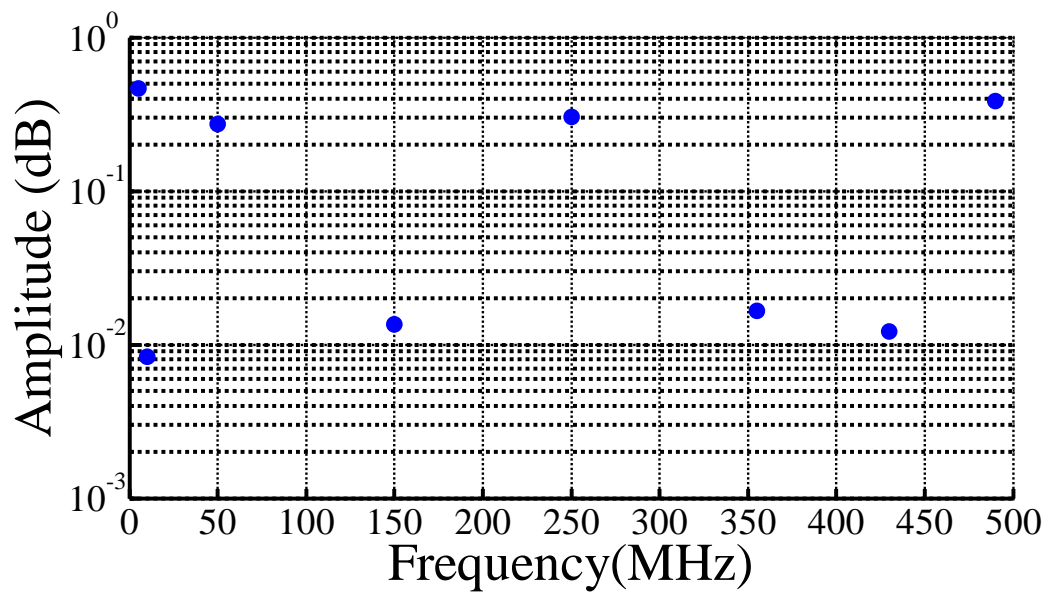


Fig.7.23 The reconstructed spectrum with the input at 50MHz, 250MHz, -490MHz

(phases shifted by 180 degree)

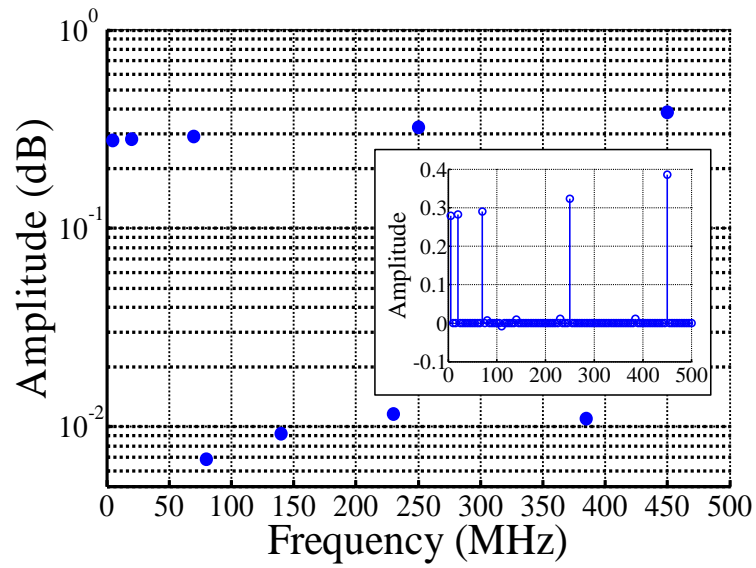


Fig.7.24 The reconstructed spectrum with the input at 20MHz, -70MHz (phases shifted by 180 degree), 250MHz, 450 MHz

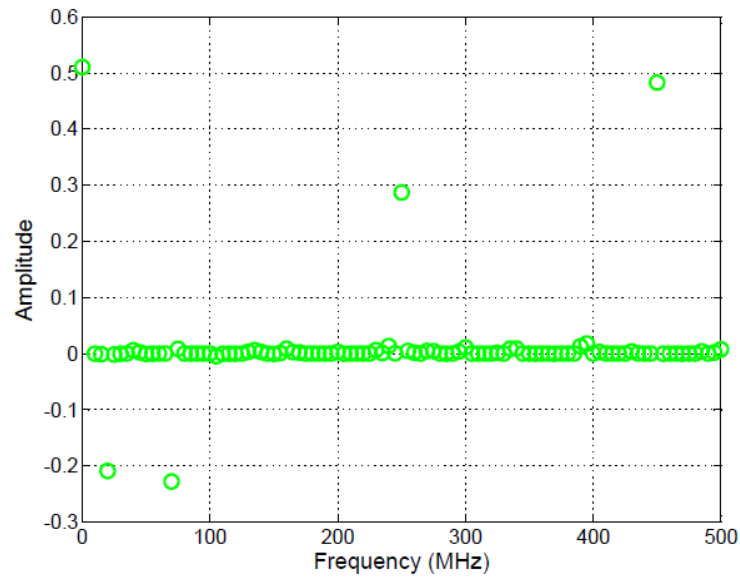


Fig.7.25 The reconstructed spectrum with the input at -20MHz (shifted 180 degree), -70MHz (shifted 180 degree), 250MHz, 450MHz



Higher frequency carriers are with higher signal amplitudes because of the pre-distortion operation (applying an internal equalizer) inside the arbitrary waveform generator N8241A. The spectrum of the 10 tones signal exiting the N8241A is shown in Fig.7.26. The spectrum is tested and calculated directly by the FFT function of the oscilloscope DSA91304A.

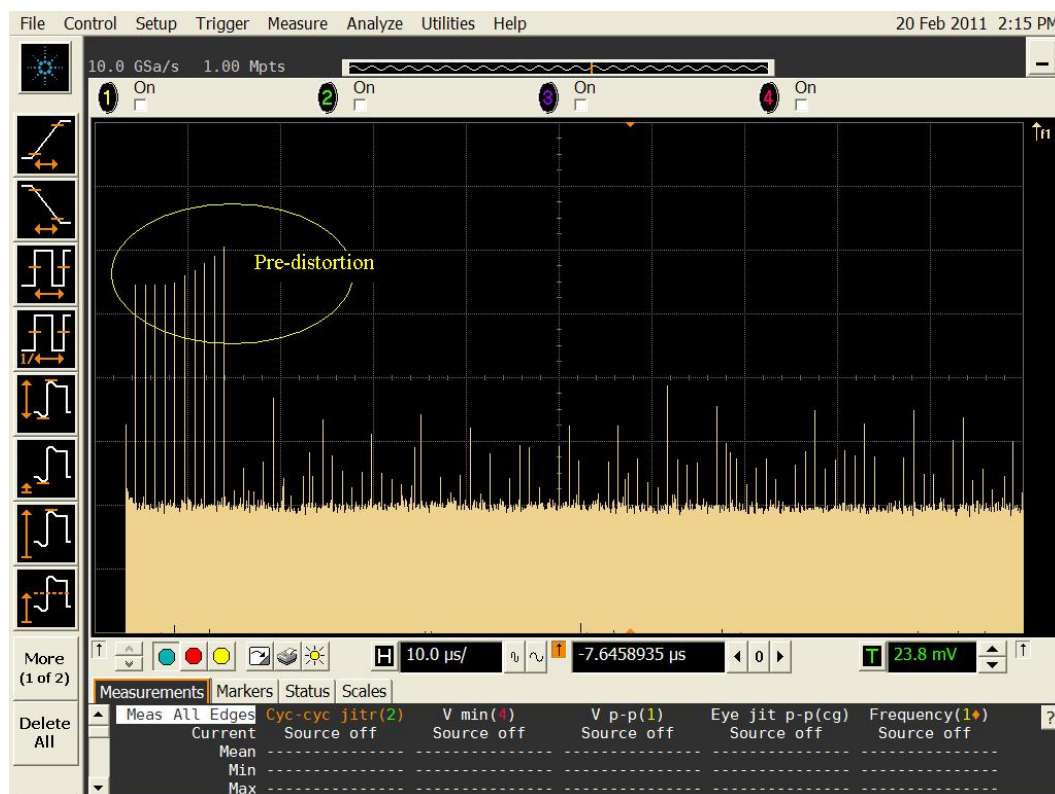


Fig.7.26 The pre-distorted spectrum of the multi-tone wideband signal exiting the

N8241A

The reconstructed SNRs with multi-tones input signals are summarized in Table 7.4.

The symbol ‘-’ represents a signal with 180 degree phase shift.

Table 7.4 Reconstructed multi-tones signals from the GHz CS system

Input Testing Signal Frequencies (Hz) and phases	Reconstructed Frequencies (Hz) and phases	Reconstructed SNR
20 M, 70 M, 250 M, 450 M	20 M, 70 M, 250 M, 450 M	27.74 dB
50 M, 250 M, 490 M	50 M, 250 M, 490 M	29.2627 dB
50 M, 150 M, 250 M, 490 M	50 M, 150 M, 250 M, 490 M	29.42 dB
50 M, 250 M, -490 M	50 M, 250 M, -490 M	29.616 dB
20 M, -70M, 250 M, 450 M	20 M, -70M, 250 M, 450 M	26.657 dB
-20 M, -70M, 250 M, 450 M	-20 M, -70M, 250 M, 450 M	24.53 dB

The reconstructed SNR is mainly limited by the 4.13 ps PN jitter. The maximum achievable SNR with the single tone test is around 40 dB. The SNR with a single tone input degrades gradually to 34 dB with the frequency increasing because the gain of the front-end rolls off at high frequency as explained in Chapter III. When multi-tones input signals are present at the input, due to the low peak-to-average value, the overall signal power is lower than the single tone input signal with the same fullscale peak-to-peak amplitude, so the input SNR as well as the reconstructed SNR is around 10 dB lower than that in single tone tests. The tested system may be considered as an A-to-D system with 6 bits ENOB and 1 GS/s sampling rate. The power consumption of the system as

well as the estimated power consumption of the ADCs is scaled down compared to that in Table 6.2 due to working at lower frequency. The overall power consumption of the tested system is around 54 mW.

d) Comparison to the state-of-art Nyquist rate data acquisition system

Simple comparison between the tested CS system and the Nyquist rate data acquisition system can be made by calculating the traditional ADCs' FOM as shown in Table 6.3. However, FOMs shown in the table didn't take into account the power consumption of the master clock generating circuit (PLL). The performance of high speed data acquisition systems significantly relies on the quality of the master clock. For example, in the time-interleaved ADC architecture, the sampling clock jitter limits the maximum achievable SNR. Also in the tested CS system, the PN jitter setups the reconstructed noise floor. Power consumption of the PLL that generates the required low jitter clock needs to be considered. The ISSCC low-jitter PLL designs demonstrate an average FOM of -230 dB [32]. The PLL's FOM is defined as below [32],

$$FOM_{PLL} = 10 \log \left[ \left( \frac{\sigma_{jitter}}{1s} \right)^2 \cdot \left( \frac{Power_{PLL}}{1mW} \right) \right] \quad (7.2)$$

In the proposed CS system, due to the signal compression, the sampler works at low frequency so the reconstructed SNR is usually not limited by the sampling jitter. The

system suffers less from the clock jitter compared to that in traditional Nyquist rate ADCs. 40 dB maximum SNR is achieved with 4.13 ps jitter variance. (7.2) suggests that the power consumption of the required PLL is below 1 mW. The power consumption of the ADC, front-end core plus the PLL is about 55 mW. The FOM of the complete data acquisition system is 0.66 pJ/conversion step. The proposed CS system achieves 44 dB ENOB with 0.5 ps jitter variance in simulation. In that case, the modified FOM is 0.41 pJ/conversion step taking into account the estimated 40 mW PLL power.

In traditional Nyquist rate sampling circuits, the signal SNR is limited by the sampling jitter [33],

$$SNR = -20\log\left(2\pi f_{signal}\sigma_{jitter}\right) \quad (7.3)$$

In reference [5], 55 dB ENOB is achieved. The maximum signal frequency is 500 MHz which is half the sampling rate. Assume that the jitter limited SNR is 60 dB, leaving reasonable margin for the thermal noise, quantization noise and distortions. According to (7.3) the required jitter variance is 0.32 ps. (7.2) suggests that the required PLL burns 97.6 mW. The overall power of the complete ADC system is 347.6 mW. The FOM of the system is 0.78 pJ/conversion step.

The modified FOMs including those of [6] and [7] are calculated and listed in table 7.5. It is shown that when the signal exhibits 4% sparsity in frequency domain, the proposed CS data acquisition system has a better FOM.



## CHAPTER VIII

### CONCLUSIONS

The Compressive Sensing theory suggests that a sparse signal may be partially compressed before the sampling. In communication applications, frequency domain sparse signal is commonly present at the input of the front-end. The sampling rate of the ADC can be lowered by compressing the incoming signal before it is sent to the ADC. According to the basic math model of Compressive Sensing theory, it is shown that the compression operation before the sampling can be implemented with front-end architecture that is similar with traditional RF receiver front-ends, except for that the local oscillator signal is replaced with a Pseudo-random number sequence. The PN sequence randomizes the spectrum of the input signal and creates the fundamental mechanism allowing a low frequency ADC to sample part of the information of the input signal at very low frequency range. The sampled data are finally sent to the following ADC and reconstructed in digital domain. Without the impact of noise and other circuit non-idealities, the signal can be perfectly reconstructed with sampling rate much lower than the Nyquist rate, enabling us to simultaneously detect the whole ultra-wide bandwidth with acceptable power consumption. In reality, the reconstructed signal SNR is limited by noise, distortion and clock jitter. Among those non-idealities, jitter variance is the most critical because the operation of the front-end strongly relies on various control clocking signals. The impact of circuit noise and distortion is different from that in conventional RF front-end due to the signal randomization. Specific equations and

design procedures should be employed to determine the circuit specifications. The prototype designed in Chapter VI achieved 7 bits resolution and 3 GS/s effective sampling rate in simulation assuming a 0.5 ps state-of-art jitter variance. In the testing, with a 4.13 ps clock jitter and 1 GS/s effective sampling rate, 40 dB maximum SNR is achieved with single tone input and 24~30 dB SNR is obtained with multi-tone input signal. Frequencies and phases of all the various input carriers are reconstructed correctly. The proposed system achieves better Figure of Merit compared with the high speed state-of-art ADCs.

A low frequency version of the CS system is also designed and implemented with discrete components in very noisy environment. It is shown that the CS reconstruction algorithm is very robust to noise's impact and there is no problem to reconstruct the correct frequencies and phases.

The PN sequences that are applied to the real circuit are distorted by the charge leakage, the finite rising/falling time and clock skews. It is difficult to calibrate those higher order errors in digital domain. Direct training method may be employed to form the reconstruction matrix that contains all the static circuit non-idealities. All the input carriers need to be transmitted through the front-end tone by tone in order to complete the training process.

The design bottle neck of the CS data acquisition system is transferred from the analog parts such as the ADCs to digital circuits such as the PN sequence generators. The speed, or data rate, of the PN sequence needs to be at least the Nyquist rate of the input signal bandwidth to avoid aliasing so the maximum input signal bandwidth is

determined by how fast the PN sequence is. Also, the jitter noise from the PN generator is also a main source that contributes to the reconstructed noise floor. Parallel PN generators may be employed to boost the data rate of the generated PN sequences. The hardware requirements on the analog parts are significantly relaxed due to the signal compression. The base band filters and the ADCs are working at low frequency and the power consumption is reduced. Almost half of the overall power consumption of the designed prototype comes from the digital clocking generators, which is supposed to shrink further in future with the technology scaling.



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## APPENDIX A

## PSEUDO-CODE FOR CS RECONSTRUCTION WITH OMP

(Definitions of  $x, s, \Phi$  and  $\psi$  are given in chapter II)

Initialization:  $\mathbf{z}_0 = s$

Iteration: for  $k = 1 : K$ , do

(1) Calculate the projection of the residue over the direction of  $\mathbf{V}_j$  for all  $j$

$$b_{k,j} = \langle \mathbf{z}_{k-1}, \mathbf{V}_j \rangle$$

where,  $\mathbf{V}_j$  is the  $j$ th column of the reconstruction matrix  $\mathbf{V} = \Phi \psi^H$

(2) Find the column  $\mathbf{V}_{i_k}$  such that

$$i_k = \arg \max b_{k,j}$$

(3) Compute the new residue  $\mathbf{z}_k$

$$\hat{a}_k = \frac{\langle \mathbf{z}_k, \mathbf{V}_{i_k} \rangle}{\langle \mathbf{V}_{i_k}, \mathbf{V}_{i_k} \rangle}$$

$$\mathbf{z}_k = \mathbf{z}_{k-1} - \hat{a}_k \mathbf{V}_{i_k}$$

Output the reconstructed signal:  $x = \sum_{k=1}^K \hat{a}_k \psi^H_{i_k}$

where,  $\psi^H_{i_k}$  is the  $i_k$ th column of  $\psi^H$ .

## APPENDIX B

### OPTIMIZATION PROBLEM FOR PSCS

In the PSCS architecture, the input signal  $x = \Psi^H y$  is fed into  $P$  parallel paths. In the  $p_{th}$  path,  $x$  is mixed with a random basis function  $\Phi_p$ . The output of the mixer is then sent to segmented timing windows with a width of  $T_i$  and integrated. The output of the integrators are sampled and  $Q$  samples are collected at each path. The  $q_{th}$  sample of the  $p_{th}$  branch is given by,

$$s_{q,p} = \int_{(q-1)T_i}^{qT_i} x \Phi_p dt.$$

There are a total of  $M = PQ$  samples collected and these samples are organized into a vector as follows,

$$s = [\tilde{s}_1^T, \tilde{s}_2^T, \dots, \tilde{s}_Q^T]^T,$$

where,  $\tilde{s}_q = [s_{q,1}, s_{q,2}, \dots, s_{q,P}]^T$  is the vector consisting of the  $q_{th}$  samples from all  $P$  branches.

The reconstruction matrix is given by,

$$\mathbf{V} = \{v_{i,j}\}_{M \times N}.$$

The element at the  $(q-1)P + p$  row and the  $n$  column is given by,

$$V_{(q-1)P+p,n} = \int_{(q-1)T_i}^{qT_i} \Psi_n^H \Phi_p dt.$$

The optimization problem for PSCS is given by,

$$y = \arg \min \|y\|_1, \quad s.t. \ s = \mathbf{V}y$$

An example of solutions is given in Appendix A.



## VITA

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